

FEATURES

- RF bandwidth to 13 GHz
- High and low speed FMCW ramp generation
- 25-bit fixed modulus allows subhertz frequency resolution
- PFD frequencies up to 110 MHz
- Sawtooth, triangular and parabolic waveform generation
- Ramp superimposed with FSK
- Ramp with 2 different sweep rates
- Ramp delay, frequency readback and interruption functions
- FSK and PSK functions
- 2.7 V to 3.6 V analog power supply
- 1.8 V digital power supply
- Programmable charge pump currents
- 3-wire serial interface
- Digital lock detect
- Power-down mode
- Cycle slip reduction for faster lock times
- 3000 V HBM/1000 V CDM ESD performance

APPLICATIONS

- FMCW radars
- Communications test equipment
- Communications infrastructure

GENERAL DESCRIPTION

The ADF4159 is a 13 GHz, fractional-N frequency synthesizer with modulation and both fast and slow waveform generation capability. It uses a 25-bit fixed modulus, allowing subhertz resolution. The part consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a sigma-delta (Σ - Δ) based fractional interpolator to allow programmable fractional-N division. The INT and FRAC registers define an overall N-divider as $N = INT + (FRAC/2^{25})$.

The ADF4159 can be used to implement frequency shift keying (FSK) and phase shift keying (PSK) modulation. There are also frequency sweep modes available that generate various waveforms in the frequency domain, for example, sawtooth and triangular waveforms. The ADF4159 features cycle slip reduction circuitry, which leads to faster lock times, without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with an analog power supply in the range of 2.7 V to 3.6 V and a digital power supply in the range of 1.6 V to 2 V. It can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

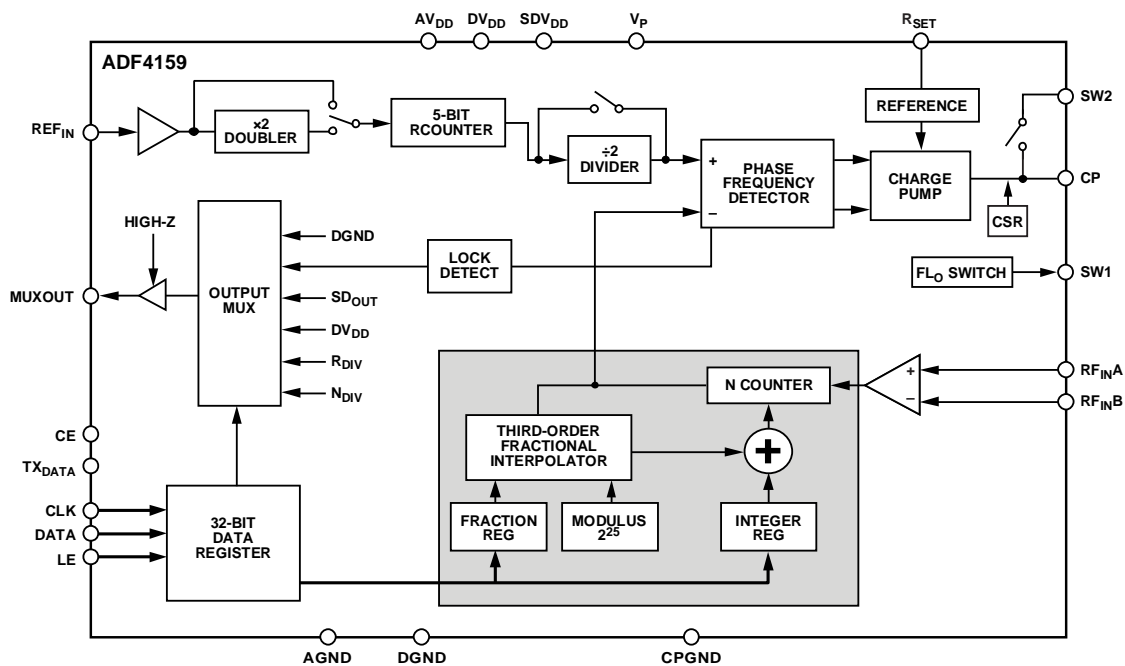


Figure 1.

Rev. PrE

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REVISION HISTORY

SPECIFICATIONS

$AV_{DD} = V_P = 2.7\text{ V to }3.6\text{ V}$, $DV_{DD} = SDV_{DD} = 1.8\text{ V}$, $AGND = DGND = 0\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , dBm referred to $50\ \Omega$, unless otherwise noted.

Table 1.

| Parameter ¹ | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----------------------|------|------|--------|---|
| RF CHARACTERISTICS | | | | | |
| RF Input Frequency (RF _{IN}) | 0.5 | | 13 | GHz | –10 dBm minimum to 0 dBm maximum; for lower frequencies, ensure slew rate (SR) ≥ 400 V/μs |
| Prescaler Output Frequency | | | 2 | GHz | For higher frequencies, use 8/9 prescaler |
| REFERENCE CHARACTERISTICS | | | | | |
| REF _{IN} Input Frequency | 10 | | 260 | MHz | For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 25 V/μs |
| REF _{IN} Input Sensitivity | | | –5 | dBm | Biased at 1.8/2 ² |
| REF _{IN} Input Capacitance | | | 1.2 | pF | |
| REF _{IN} Input Current | | | ±100 | μA | |
| PHASE DETECTOR | | | | | |
| Phase Detector Frequency ³ | | | 110 | MHz | |
| CHARGE PUMP | | | | | |
| I _{CP} Sink/Source | | | | | Programmable |
| High Value | | 4.75 | | mA | With R _{SET} = 5.1 kΩ |
| Low Value | | 297 | | μA | |
| Absolute Accuracy | | 2.5 | | % | With R _{SET} = 5.1 kΩ |
| R _{SET} Range | 4.59 | 5.1 | 5.61 | kΩ | |
| I _{CP} Three-State Leakage Current | | 1 | | nA | Sink and source current |
| Matching | | 2 | | % | 0.5 V < V _{CP} < V _P – 0.5 V |
| I _{CP} vs. V _{CP} | | 2 | | % | 0.5 V < V _{CP} < V _P – 0.5 V |
| I _{CP} vs. Temperature | | 2 | | % | V _{CP} = V _P /2 |
| LOGIC INPUTS | | | | | |
| V _{INH} , Input High Voltage | 1.4 | | | V | |
| V _{INL} , Input Low Voltage | | | 0.4 | V | |
| I _{INH} /I _{INL} , Input Current | | | ±1 | μA | |
| C _{IN} , Input Capacitance | | | 10 | pF | |
| LOGIC OUTPUTS | | | | | |
| V _{OH} , Output High Voltage | V _{DD} – 0.4 | | | V | CMOS output chosen |
| I _{OH} , Output High Current | | | 100 | μA | |
| V _{OL} , Output Low Voltage | | | 0.3 | V | I _{OL} = 500 μA |
| POWER SUPPLIES | | | | | |
| AV _{DD} | 2.7 | | 3.6 | V | |
| DV _{DD} , SDV _{DD} | 1.6 | 1.8 | 2 | V | |
| V _P | 2.7 | | 3.6 | V | |
| AI _{DD} | | 26 | 40 | mA | Supply current drawn by AV _{DD} |
| DI _{DD} | | 6 | 8 | mA | Supply current drawn by DV _{DD} |
| I _P | | 3 | 4 | mA | Supply current drawn by V _P |
| Power-Down Mode | | 2 | | μA | |
| NOISE CHARACTERISTICS | | | | | |
| Normalized Phase Noise Floor ⁴ | | –224 | | dBc/Hz | PLL loop BW = 1 MHz |
| Normalized 1/f Noise (PN _{1..t}) ⁵ | | –120 | | dBc/Hz | Measured at 10 kHz offset, normalized to 1 GHz |
| Phase Noise Performance ⁶ | | | | | At VCO output |
| 12002 MHz Output ⁷ | | –96 | | dBc/Hz | At 50 kHz offset, 100 MHz PFD frequency |

¹ Operating temperature: –40°C to +125°C.

² AC-coupling ensures 1.8/2 bias.

³ Guaranteed by design. Sample tested to ensure compliance.

⁴ This figure can be used to calculate phase noise for any application. Use the formula ((Normalized Phase Noise Floor) + 10 log(f_{PFD}) + 20 logN) to calculate in-band phase noise performance as seen at the VCO output.

⁵ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF} , and at an offset frequency, f , is given by $PN = P_{1/f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

⁶ The phase noise is measured with the EV-ADF4159EB1Z and the Rohde & Schwarz FSUP signal source analyzer.

⁷ $f_{REFIN} = 100 \text{ MHz}$; $f_{PFD} = 100 \text{ MHz}$; offset frequency = 50 kHz; $RF_{OUT} = 12002 \text{ MHz}$; $N = 120.02$; loop bandwidth = 250 kHz.

TIMING SPECIFICATIONS

$AV_{DD} = V_P = 2.7 \text{ V to } 3.6 \text{ V}$; $DV_{DD} = SDV_{DD} = 1.8 \text{ V}$; $AGND = DGND = SDGND = 0 \text{ V}$; $T_A = T_{MIN} \text{ to } T_{MAX}$, dBm referred to 50 Ω , unless otherwise noted.

Table 2. Write Timing

| Parameter | Limit at T_{MIN} to T_{MAX} | Unit | Test Conditions/Comments |
|-----------|---------------------------------|--------|--------------------------|
| t_1 | 20 | ns min | LE setup time |
| t_2 | 10 | ns min | DATA to CLK setup time |
| t_3 | 10 | ns min | DATA to CLK hold time |
| t_4 | 25 | ns min | CLK high duration |
| t_5 | 25 | ns min | CLK low duration |
| t_6 | 10 | ns min | CLK to LE setup time |
| t_7 | 20 | ns min | LE pulse width |

Write Timing Diagram

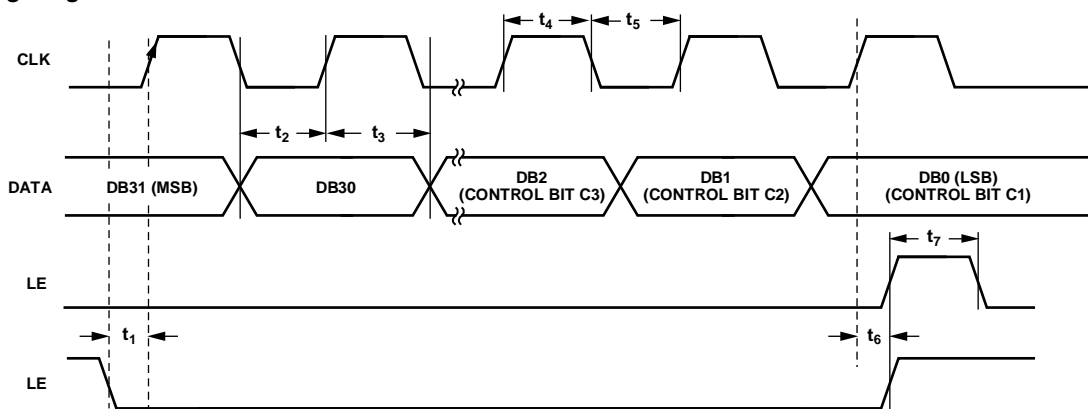


Figure 2. Write Timing Diagram

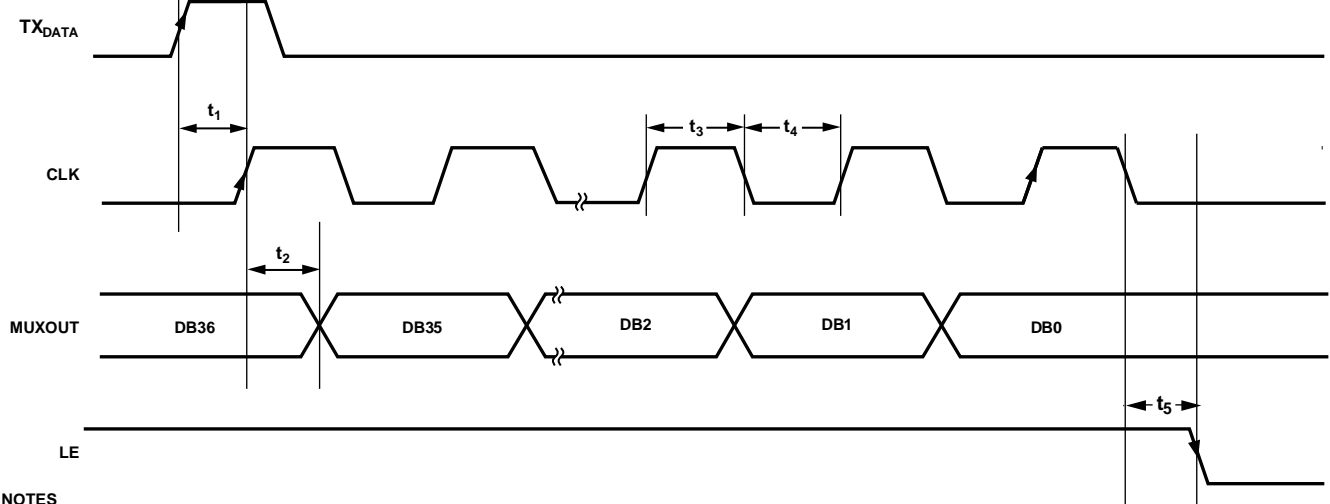
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Table 3. Read Timing

| Parameter | Limit at T _{MIN} to T _{MAX} | Unit | Test Conditions/Comments |
|-----------------------------|---|--------|------------------------------------|
| t ₁ ¹ | t _{PFD} + 20 | ns min | TX _{DATA} setup time |
| t ₂ | 20 | ns min | CLK setup time to DATA (on MUXOUT) |
| t ₃ | 25 | ns min | CLK high duration |
| t ₄ | 25 | ns min | CLK low duration |
| t ₅ | 10 | ns min | CLK to LE setup time |

¹ t_{PFD} is period of the PFD frequency, for example, if PFD frequency is 50 MHz, t_{PFD} = 20 ns.

Read Timing Diagram



NOTES
1. LE SHOULD BE KEPT HIGH DURING READBACK.

Figure 3. Read Timing Diagram

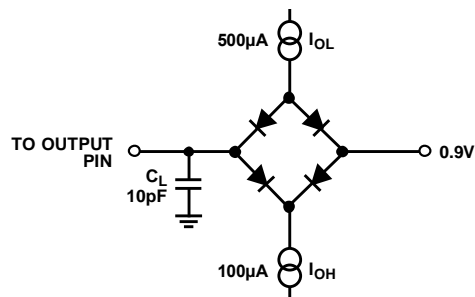


Figure 4. Load Circuit for MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, $\text{GND} = \text{AGND} = \text{DGND} = \text{SDGND} = 0\text{ V}$,
 $V_{DD} = AV_{DD} = V_P$, $DV_{DD} = SDV_{DD}$, unless otherwise noted.

Table 4.

| Parameter | Rating |
|--|------------------------------------|
| AV_{DD} to GND | -0.3 V to +3.9 V |
| DV_{DD} to GND | -0.3 V to +2.4 V |
| V_P to GND | -0.3 V to +3.9 V |
| V_P to AV_{DD} | -0.3 V to +0.3 V |
| Digital I/O Voltage to GND | -0.3 V to $DV_{DD} + 0.3\text{ V}$ |
| Analog I/O Voltage to GND | -0.3 V to $V_{DD} + 0.3\text{ V}$ |
| REF_{IN} to GND | -0.3 V to $DV_{DD} + 0.3\text{ V}$ |
| RF_{IN} to GND | -0.3 V to $V_{DD} + 0.3\text{ V}$ |
| Operating Temperature Range | |
| Industrial | -40°C to +125°C |
| Storage Temperature Range | -65°C to +125°C |
| Maximum Junction Temperature | 150°C |
| LFCSP θ_{JA} Thermal Impedance (Paddle Soldered) | 30.4°C/W |
| Reflow Soldering | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 40 sec |
| ESD (Charged Device Model) | 1000 V |
| ESD (Human Body Model) | 3000 V |

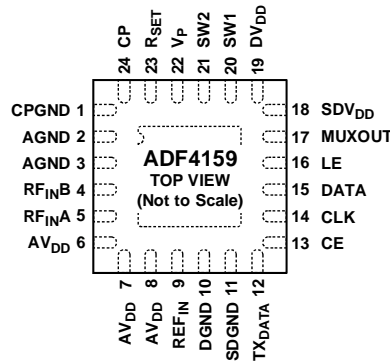
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS



- NOTES**
1. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE CONNECTED TO AGND.
 2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

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Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|--------------------|---|
| 1 | CPGND | Charge Pump Ground. This is the ground return path for the charge pump. |
| 2, 3 | AGND | Analog Ground. This is the ground return path of the prescaler. |
| 4 | RF _{IN} B | Complementary Input to the RF Prescaler. Decouple this pin to the ground plane with a small bypass capacitor, typically 100 pF. |
| 5 | RF _{IN} A | Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO. |
| 6, 7, 8 | AV _{DD} | Positive Power Supply for the RF Section. Place decoupling capacitors to the ground plane as close as possible to this pin. |
| 9 | REF _{IN} | Reference Input. This is a CMOS input with a nominal threshold of V _{DD} /2 and an equivalent input resistance of 100 kΩ. It can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled. |
| 10 | DGND | Digital Ground. |
| 11 | SDGND | Digital Σ-Δ Modulator Ground. Ground return path for the Σ-Δ modulator. |
| 12 | TX _{DATA} | TX _{DATA} Pin. Provides data to be transmitted in FSK or PSK mode on this pin. Controls some ramping functionality. |
| 13 | CE | Chip Enable (1.8 V logic). A logic low on this pin powers down the device and puts the charge pump output into three-state mode. |
| 14 | CLK | Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the input shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 15 | DATA | Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input. |
| 16 | LE | Load Enable, CMOS Input. When LE is high, the data stored in the input shift register is loaded into one of the eight latches, with the latch being selected using the control bits. |
| 17 | MUXOUT | Multiplexer Output. This pin allows various internal signals to be accessed externally. |
| 18 | SDV _{DD} | Power Supply Pin for the Digital Σ-Δ Modulator. This pin must be 1.8 V. Place decoupling capacitors to the ground plane as close as possible to this pin. |
| 19 | DV _{DD} | Positive Power Supply for the Digital Section. Place decoupling capacitors to the digital ground plane as close as possible to this pin. DV _{DD} must be 1.8 V. |
| 20, 21 | SW1, SW2 | Switches for Fast Lock. |
| 22 | V _p | Charge Pump Power Supply. This pin must be greater than or equal to V _{DD} . The max value of V _p is 3.6 V. |
| 23 | R _{SET} | Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I _{CP} and R _{SET} is $I_{CPmax} = \frac{24.225}{R_{SET}}$ where I _{CPmax} = 4.75 mA and R _{SET} = 5.1 kΩ. |
| 24 | CP | Charge Pump Output. When enabled, this provides ±I _{CP} to the external loop filter, which, in turn, drives the external VCO. |

| | | |
|----|------|--|
| 25 | EPAD | Exposed Paddle. The LFCSP has an exposed paddle that must be connected to GND. |
|----|------|--|

TYPICAL PERFORMANCE CHARACTERISTICS

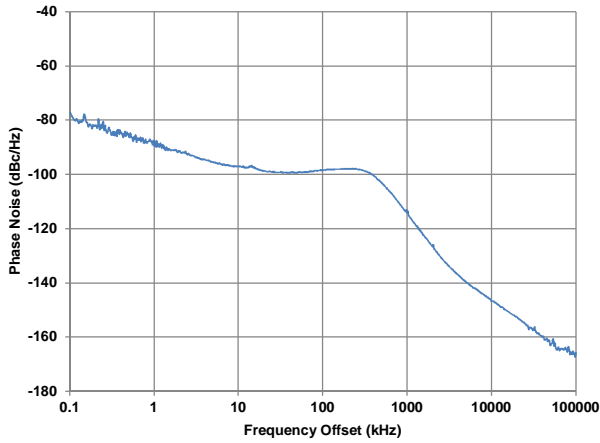


Figure 6. Phase Noise at 12.002 GHz, $F_{PFD} = 100$ MHz, Loop Bandwidth = 250 kHz, $I_{CP} = 2.5$ mA, Bleed 11.6 μ A enabled.

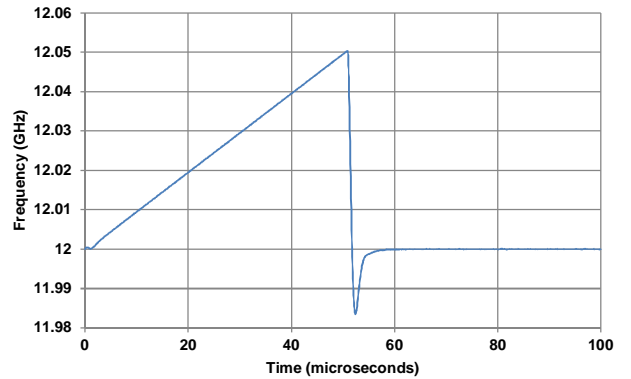


Figure 9. Sawtooth burst. $F_{PFD} = 100$ MHz, $I_{CP} = 2.5$ mA, Loop Bandwidth = 250 kHz, $CLK_1 = 3$, $CLK_2 = 26$, DEV = 1024, DEV_OFFSET = 8, Number of steps = 64.

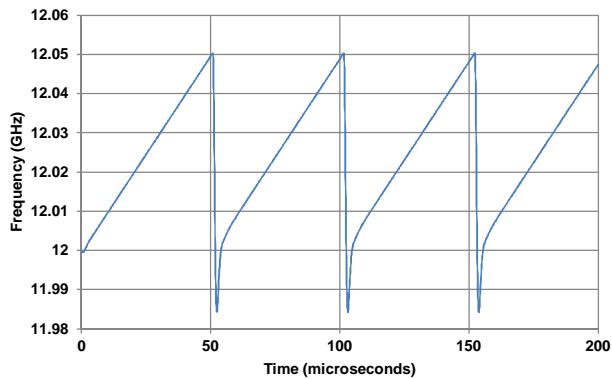


Figure 7. Sawtooth ramp. $F_{PFD} = 100$ MHz, $I_{CP} = 2.5$ mA, Loop Bandwidth = 250 kHz, $CLK_1 = 3$, $CLK_2 = 26$, DEV = 1024, DEV_OFFSET = 8, Number of steps = 64.

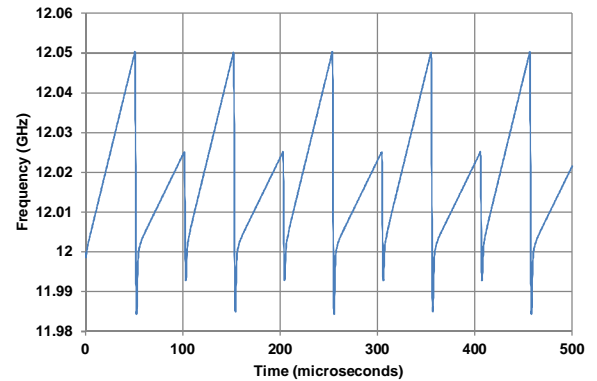


Figure 10. Dual Sawtooth Ramp. $F_{PFD} = 100$ MHz, $I_{CP} = 2.5$ mA, Loop Bandwidth = 250 kHz, $CLK_1 = 3$, $CLK_2 = 26$, DEV = 1024, DEV_OFFSET = 8, Number of steps = 64. 2nd Ramp: $CLK_2 = 52$, DEV = 1024, DEV_OFFSET = 7.

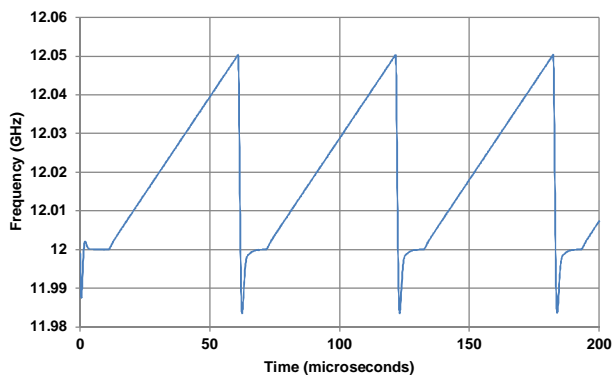


Figure 8. Sawtooth ramp with delay. $F_{PFD} = 100$ MHz, $I_{CP} = 2.5$ mA, Loop Bandwidth = 250 kHz, $CLK_1 = 3$, $CLK_2 = 26$, DEV = 1024, DEV_OFFSET = 8, Number of steps = 64, Delay word = 1000

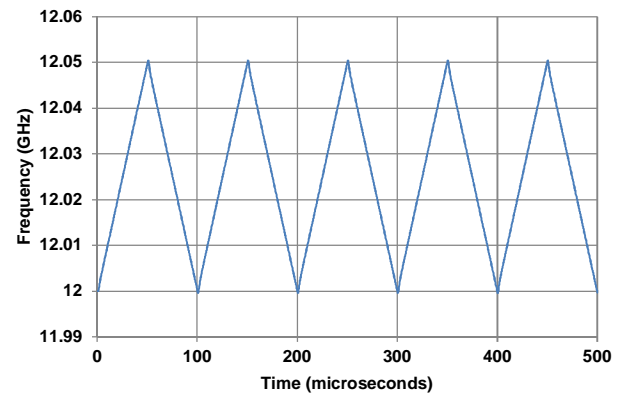


Figure 11. Triangle Ramp. $F_{PFD} = 100$ MHz, $I_{CP} = 2.5$ mA, Loop Bandwidth = 250 kHz, $CLK_1 = 3$, $CLK_2 = 26$, DEV = 1024, DEV_OFFSET = 8, Number of steps = 64

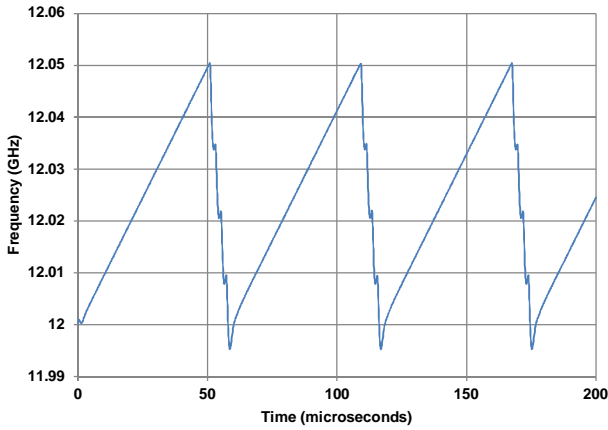


Figure 12. Fast Ramp (Triangle ramp with different slopes). $F_{\text{PFD}} = 100 \text{ MHz}$, $I_{\text{CP}} = 2.5 \text{ mA}$, Loop Bandwidth = 250 kHz, $\text{CLK}_1 = 3$, $\text{CLK}_2 = 26$, $\text{DEV} = 1024$, $\text{DEV_OFFSET} = 8$, Number of steps = 64. Down ramp: $\text{CLK}_2 = 70$, $\text{DEV} = 16384$, $\text{DEV_OFFSET} = 8$, Number of steps = 4.

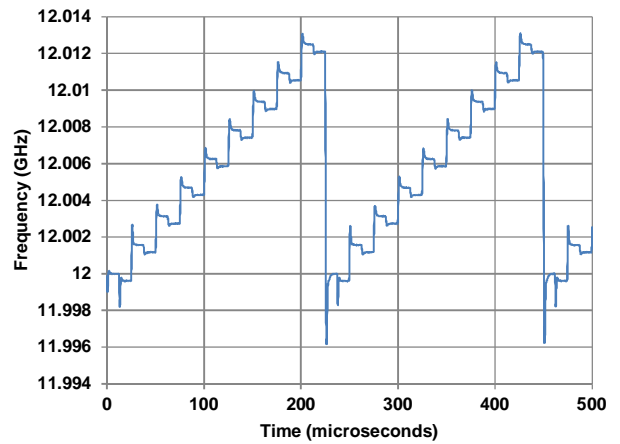


Figure 15. FSK Ramp. $F_{\text{PFD}} = 100 \text{ MHz}$, $I_{\text{CP}} = 2.5 \text{ mA}$, Loop Bandwidth = 250 kHz, $\text{CLK}_1 = 3$, $\text{CLK}_2 = 26$, $\text{DEV} = 1024$, $\text{DEV_OFFSET} = 8$, Number of steps = 64. FSK: $\text{DEV} = -512$, $\text{DEV_OFFSET} = 8$.

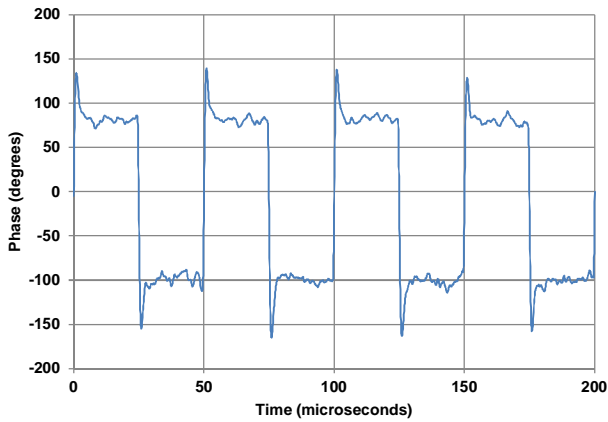


Figure 13 PSK. Loop Bandwidth = 250 kHz, $\text{DEV} = 1049$, $\text{DEV_OFFSET} = 9$, Data Rate = 20 kHz

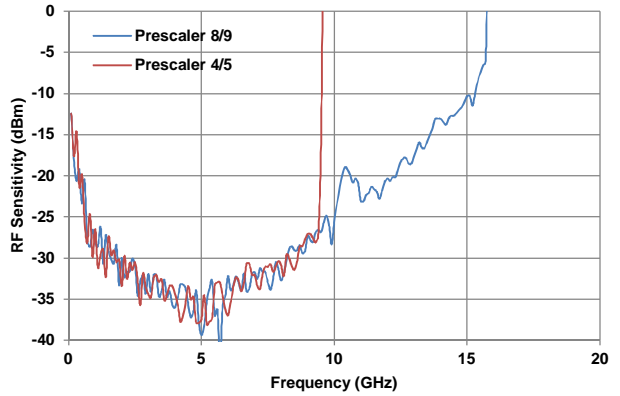


Figure 16 RF_{IN} Sensitivity at Nominal Temperature

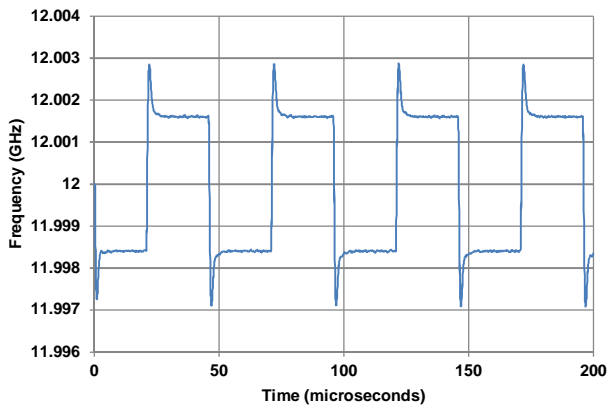


Figure 14. FSK. Loop Bandwidth = 250 kHz, $\text{DEV} = 1049$, $\text{DEV_OFFSET} = 9$, Data Rate = 20 kHz

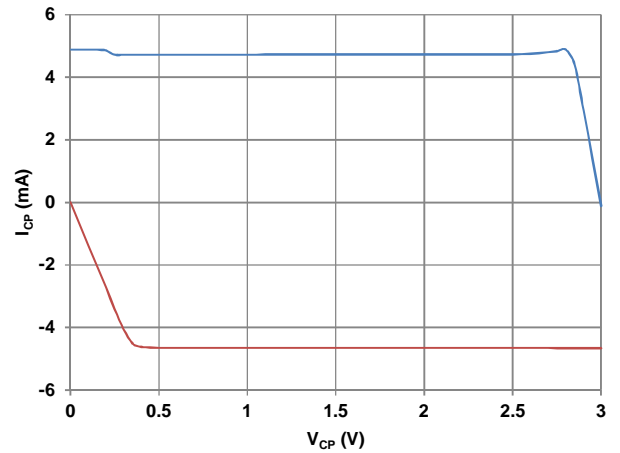


Figure 17. Charge Pump Output Characteristics

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 18. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

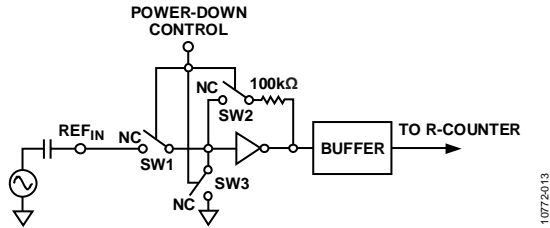


Figure 18. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 19. It is followed by a two-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

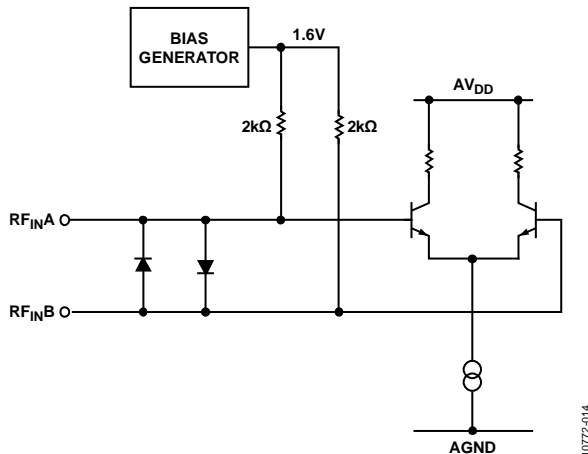


Figure 19. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

25-BIT FIXED MODULUS

The ADF4159 has a 25-bit fixed modulus. This allows output frequencies to be spaced with a resolution of

$$f_{RES} = f_{PFD} / 2^{25} \quad (1)$$

where f_{PFD} is the frequency of the phase frequency detector (PFD). For example, with a PFD frequency of 100 MHz, frequency steps of 2.98 Hz are possible.

INT, FRAC AND R RELATIONSHIP

The INT and FRAC values in conjunction with the R-counter make it possible to generate output frequencies that are spaced by fractions of the PFD. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (2)$$

where:

RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

INT is the preset divide ratio of the binary 12-bit counter (23 to 4095).

FRAC is the numerator of the fractional division (0 to (2²⁵ - 1)).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (3)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit (0 or 1).

T is the REF_{IN} divide-by-2 bit (0 or 1).

R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

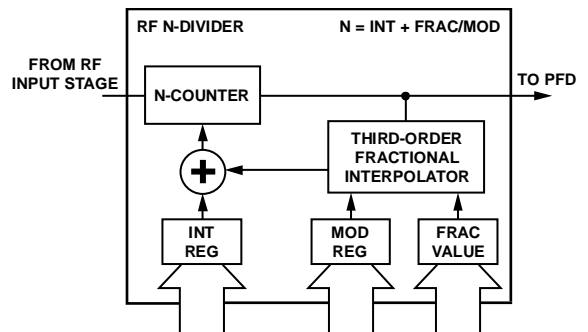


Figure 20. RF N-Divider

R-COUNTER

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R-counter and N-counter and produces an output proportional to the phase and frequency difference between them. Figure 21 shows a simplified schematic of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

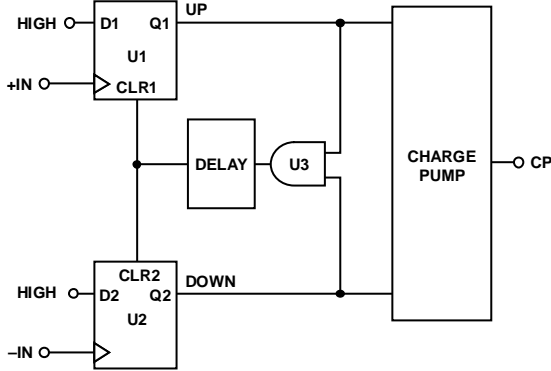


Figure 21. PFD Simplified Schematic

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MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4159 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M4, M3, M2, and M1 bits (see Figure 25). Figure 22 shows the MUXOUT section in block diagram form.

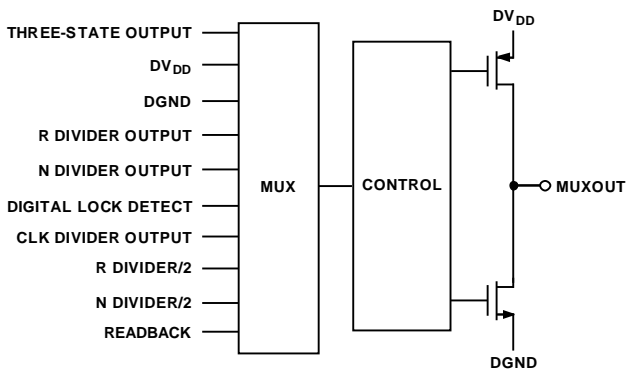


Figure 22. MUXOUT Schematic

10772-017

INPUT SHIFT REGISTER

The ADF4159 digital section includes a 5-bit RF R-counter, a 12-bit INT-counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of eight latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the input shift register. These are the three LSBs (DB2, DB1, and DB0, respectively), as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 23 and Figure 24 show a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 25 through Figure 32 show how to set up the program modes in the ADF4159.

Several settings in the ADF4159 are double buffered. These include the LSB fractional value, R-counter value, reference doubler, current setting, CLK₁ divider, and RDIV2. This means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, updating the fractional value can involve a write to the 13 LSB bits in R1 and the 12 MSB bits in R0. R1 must be written to first, followed by the write to R0. The frequency change begins after the write to R0. Double buffering ensures that the bits written to in R1 do not take effect until after the write to R0.

Table 6. C3, C2, and C1 Truth Table

| Control Bits | | | Register |
|--------------|----|----|----------|
| C3 | C2 | C1 | |
| 0 | 0 | 0 | R0 |
| 0 | 0 | 1 | R1 |
| 0 | 1 | 0 | R2 |
| 0 | 1 | 1 | R3 |
| 1 | 0 | 0 | R4 |
| 1 | 0 | 1 | R5 |
| 1 | 1 | 0 | R6 |
| 1 | 1 | 1 | R7 |

REGISTER MAPS

FRAC/INT REGISTER (R0)

| RAMP ON | MUXOUT CONTROL | | | | | 12-BIT INTEGER VALUE (INT) | | | | | | | | | | 12-BIT MSB FRACTIONAL VALUE (FRAC) | | | | | | | | | | CONTROL BITS | | | | | |
|---------|----------------|------|------|------|------|----------------------------|------|------|------|------|------|------|------|------|------|------------------------------------|------|------|------|------|------|------|-----|-----|-----|--------------|-----|-----|-------|-------|-------|
| | DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 |
| R1 | M4 | M3 | M2 | M1 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | F25 | F24 | F23 | F22 | F21 | F20 | F19 | F18 | F17 | F16 | F15 | F14 | C3(0) | C2(0) | C1(0) |

LSB FRAC REGISTER (R1)

| RESERVED | | | | PHASE ADJUST | 13-BIT LSB FRACTIONAL VALUE (FRAC) | | | | | | | | | | | | 12-BIT PHASE VALUE | | | | | | | | | | | | CONTROL BITS | | | | | |
|----------|------|------|------|--------------|------------------------------------|------|------|------|------|------|------|------|------|------|------|------|--------------------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------------|-----|-----|-------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 0 | 0 | 0 | 0 | P1 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | C3(0) | C2(0) | C1(1) |

R-DIVIDER REGISTER (R2)

| RESERVED | | | | CSR | CURRENT SETTING | | | | | RESERVED | PRESCALER | R DIV2 DBB | REFERENCE DOUBLER DBB | 5-BIT R-COUNTER | | | | | 12-BIT CLK ₁ DIVIDER (DBB) | | | | | | | | | | CONTROL BITS | | | |
|----------|------|------|------|-----|-----------------|------|------|------|------|----------|-----------|------------|-----------------------|-----------------|------|------|------|------|---------------------------------------|------|------|------|------|------|------|------|-----|-----|--------------|-------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | | DB27 | DB26 | DB25 | DB24 | DB23 | | | | | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 |
| 0 | 0 | 0 | 0 | CR1 | CPI4 | CPI3 | CPI2 | CPI1 | 0 | P1 | U2 | U1 | R5 | R4 | R3 | R2 | R1 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | C3(0) | C2(1) | C1(0) |

FUNCTION REGISTER (R3)

| RESERVED | | | | | | | | | | NEG BLEED CURRENT | | | NEG BLEED EN | RESERVED | CHARGE CANCELLATION | RESERVED | ABP | LOL | N SEL | SD RESET | RESERVED | RAMP MODE | | PSK | FSK | LDP | PD POLARITY | PD | CP THREE-STATE COUNTER RESET | CONTROL BITS | | |
|----------|------|------|------|------|------|------|------|------|------|-------------------|------|------|--------------|----------|---------------------|----------|-----|-----|-------|----------|----------|-----------|------|-----|-----|-----|-------------|----|------------------------------|--------------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | | | | | | | | | | DB18 | DB17 | | | | | | | DB16 | DB15 | DB14 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NB3 | NB2 | NB1 | 0 | 0 | 0 | 0 | 1 | L1 | NS1 | U12 | 0 | 0 | RM2 | RM1 | 0 | 0 | U11 | U10 | U9 | U8 | U7 | C3(0) | C2(1) | C1(1) |

NOTES
1. DBB = DOUBLE BUFFERED BIT(S).

Figure 23. Register Summary 1

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TEST REGISTER (R4)

| LE SEL | RESERVED | | | | | | | | RAMP STATUS | CLK DIV MODE | 12-BIT CLOCK DIVIDER VALUE | | | | | | | | | | | | CLK DIV SEL | RESERVED | | | CONTROL BITS | | | | |
|--------|----------|------|------|------|------|------|------|------|-------------|--------------|----------------------------|------|------|------|------|------|------|------|------|------|------|-----|-------------|----------|-----|-----|--------------|-----|-------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| LS1 | 0 | 0 | 0 | 0 | 0 | T5 | T4 | T3 | T2 | T1 | C2 | C1 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | CS1 | 0 | 0 | 0 | C3(1) | C2(0) | C1(0) |

DEVIATION REGISTER (R5)

| RESERVED | TXDATA INVERT | TX RAMP CLK | PARABOLIC RAMP | INTERRUPT | FSK RAMP | DUAL RAMP | DEV SEL | 4-BIT DEV OFFSET WORD | | | | 16-BIT DEVIATION WORD | | | | | | | | | | | | | | | | CONTROL BITS | | | |
|----------|---------------|-------------|----------------|-----------|----------|-----------|---------|-----------------------|------|------|------|-----------------------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------------|-------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | TR1 | 0 | I2 | I1 | 0 | 0 | DS1 | DO4 | DO3 | DO2 | DO1 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | C3(1) | C2(0) | C1(1) |

STEP REGISTER (R6)

| RESERVED | | | | | | | | STEP SEL | 20-BIT STEP WORD | | | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
|----------|------|------|------|------|------|------|------|----------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------------|-------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSE1 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S9 | S8 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | C3(1) | C2(1) | C1(0) |

DELAY REGISTER (R7)

| RESERVED | | | | | | | | TXDATA TRIGGER DELAY | TRI DELAY | SING FULL TRI | TXDATA TRIGGER | FAST RAMP | RAMP DEL FL | RAMP DEL | DEL CLK SEL | DEL START EN | 12-BIT DELAY START WORD | | | | | | | | | | | | CONTROL BITS | | |
|----------|------|------|------|------|------|------|------|----------------------|-----------|---------------|----------------|-----------|-------------|----------|-------------|--------------|-------------------------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|--------------|-------|-------|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TD1 | ST1 | TR1 | FR1 | 0 | RD1 | DC1 | DSE1 | DS12 | DS11 | DS10 | DS9 | DS8 | DS7 | DS6 | DS5 | DS4 | DS3 | DS2 | DS1 | C3(1) | C2(1) | C1(1) |

NOTES
1. DBB = DOUBLE BUFFERED BIT(S).

Figure 24. Register Summary 2

10849-019

FRAC/INT REGISTER (R0) MAP

With DB[2:0] set to 000, the on-chip FRAC/INT register, Register R0, is programmed as shown in Figure 25.

Ramp On

Setting DB31 to 1 enables the ramp. Setting DB31 to 0 disables the ramp.

MUXOUT Control

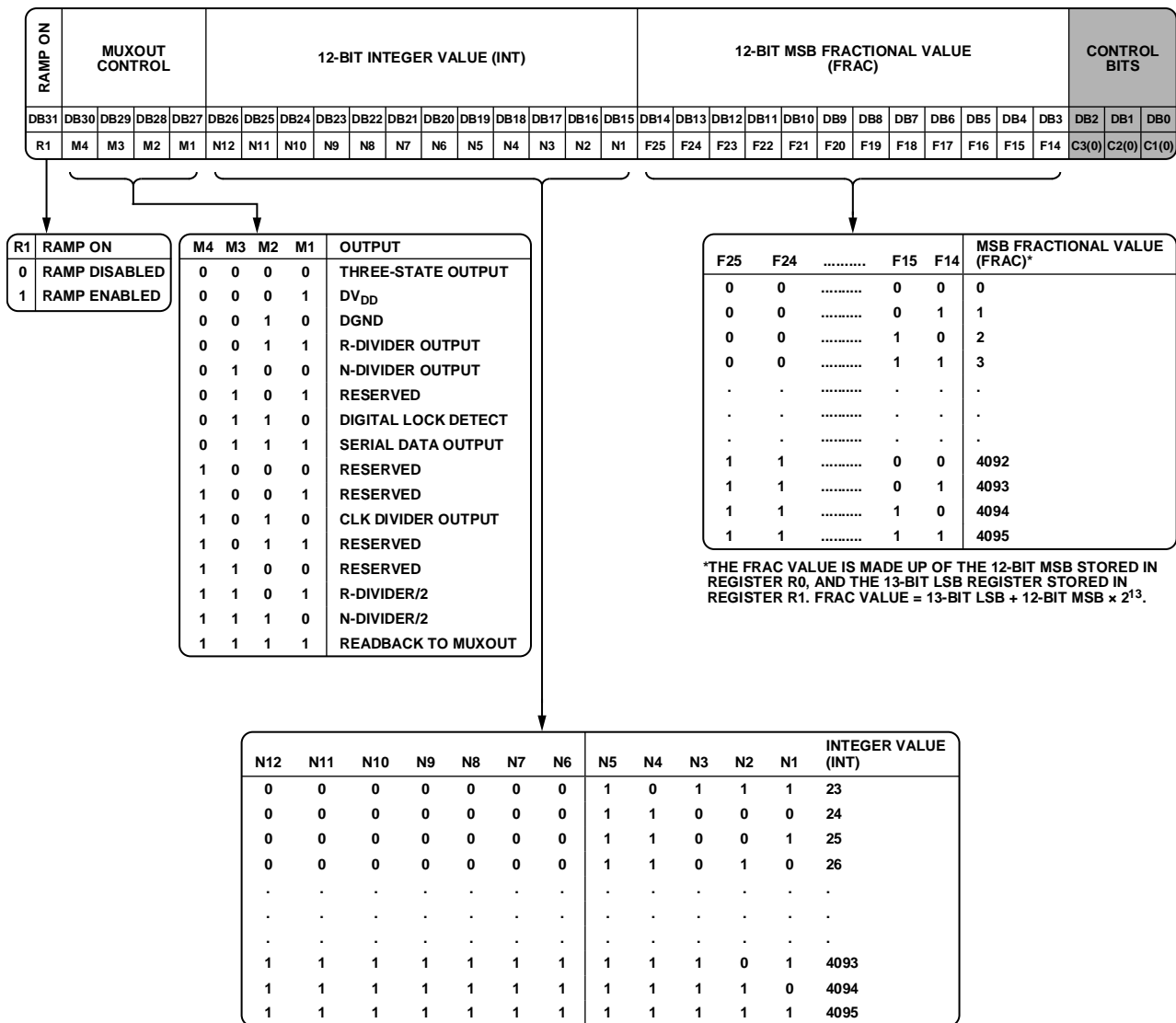
The on-chip multiplexer is controlled by DB[30:27] on the ADF4159. See Figure 25 for the truth table.

12-Bit Integer Value (INT)

These 12 bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 2. See the INT, FRAC and R Relationship section for more information.

12-Bit MSB Fractional Value (FRAC)

These 12 bits, along with Bits DB[27:15] in the LSB FRAC register (Register R1), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits DB[27:15] in the LSB FRAC register (Register R1) are the least significant bits (LSB). See the RF Synthesizer: A Worked Example section for more information.



*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER R1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2¹³.

Figure 25. FRAC/INT Register (R0) Map

LSB FRAC REGISTER (R1) MAP

With DB[2:0] set to 001, the on-chip LSB FRAC register (Register R1) is programmed as shown in Figure 26.

Phase Adj

The bit enables/disables phase adjustment. Phase of the generated by the value programmed in DB[14:3] of Register R1 (12 Bit Phase Value).

13-Bit LSB FRAC Value

These 13 bits, along with Bits DB[14:3] in the FRAC/INT register (Register R0), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 13 bits are the least significant bits (LSB) of the 25-bit

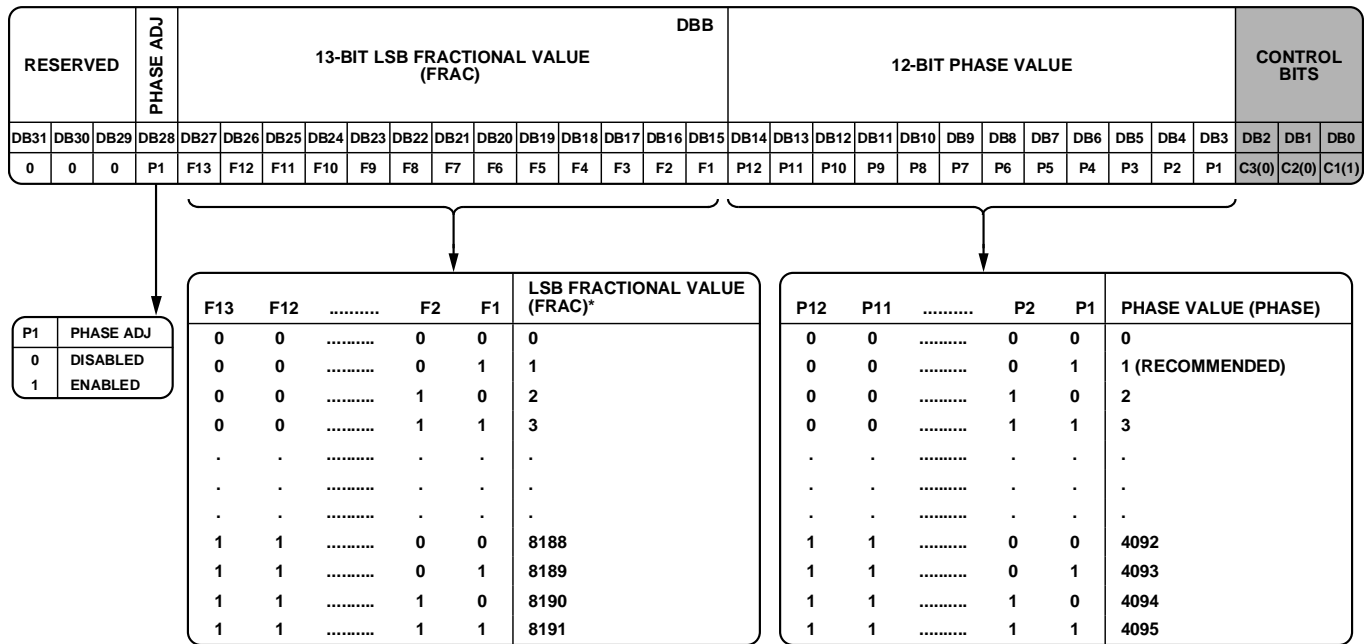
FRAC value, and Bits DB[14:3] in the INT/FRAC register are the most significant bits (MSB). See the RF Synthesizer: A Worked Example section for more information.

12-Bit Phase Value

These 12 bits control what is loaded as the Phase word. The word is used to program the RF output phase from 0° to 360° with a resolution of 360°/2¹². The phase shift equals to (Phase Value × 360°) / 2¹². If the Phase Adjustment is not being used, it is recommended that the Phase Value be set to 0.

Reserved Bits

All reserved bits must be set to 0 for normal operation.



*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER R1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2¹³.

NOTES
1. DBB = DOUBLE BUFFERED BIT(S).

Figure 26. LSB FRAC Register (R1) Map

10849-021

R-DIVIDER REGISTER (R2) MAP

With DB[2:0] set to 010, the on-chip R-divider register (Register R2) is programmed as shown in Figure 27.

Reserved Bits

All reserved bits must be set to 0 for normal operation.

CSR Enable

Setting this bit to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the PFD must have a 50% duty cycle in order for cycle slip reduction to work. In addition, the charge pump current setting must be set to a minimum. See the **Error! Reference source not found.** section on Page 23 for more information.

Also note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is set to negative.

Charge Pump Current Setting

DB[27:24] set the charge pump current setting (see Figure 27). Set these bits to the charge pump current that the loop filter is designed with.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and fixed modulus counters, determine the overall division ratio from RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 8 GHz. Therefore, when operating the [ADF4159](#) at frequencies greater than 8 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value.

With $P = 4/5$, $N_{MIN} = 23$

With $P = 8/9$, $N_{MIN} = 75$

RDIV2

Setting DB21 to 1 inserts a divide-by-2 toggle flip-flop between the R-counter and the PFD. This can be used to provide a 50% duty cycle signal at the PFD.

Reference Doubler

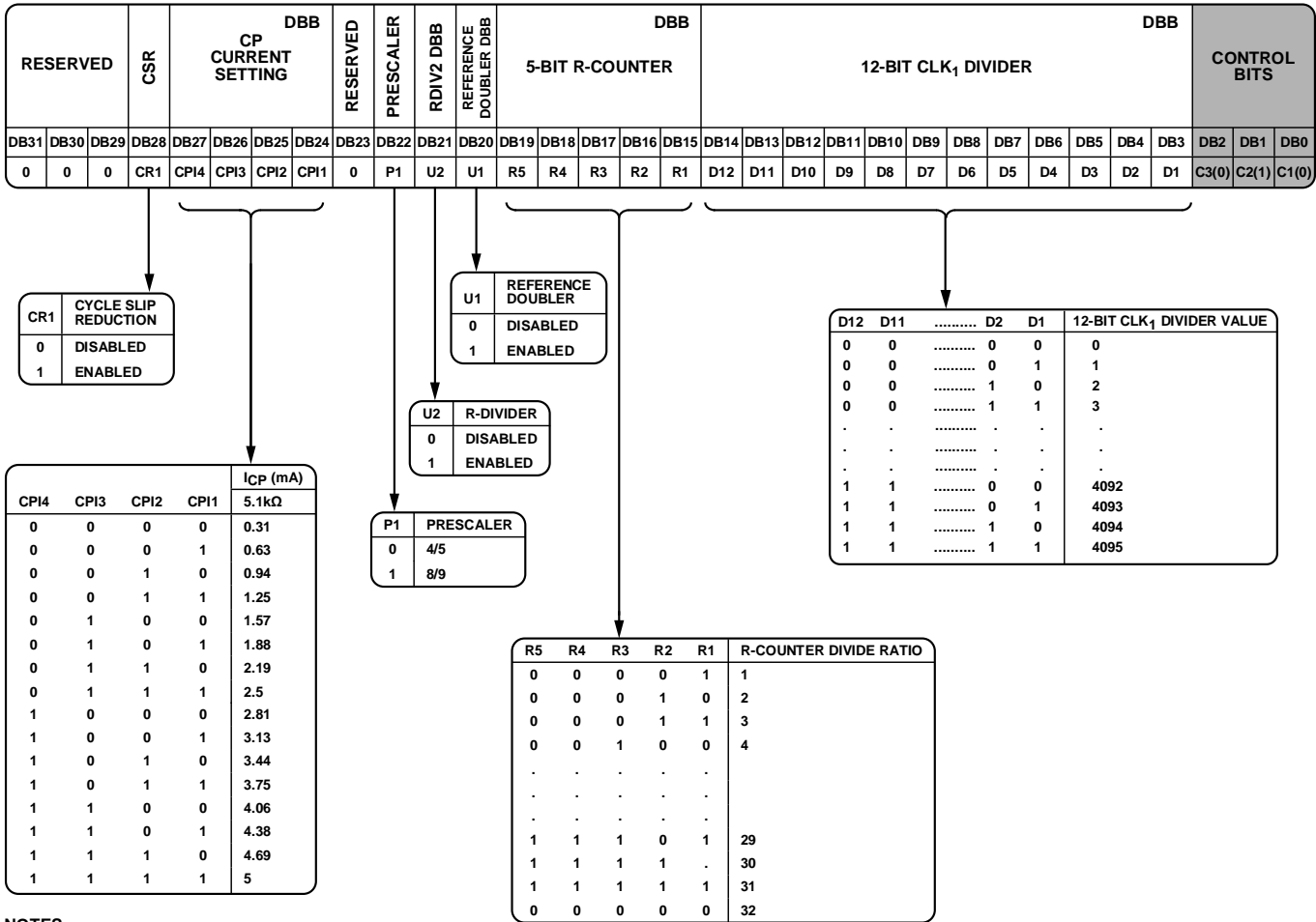
Setting DB20 to 0 feeds the REF_{IN} signal directly to the 5-bit RF R-counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding the signal into the 5-bit R-counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising edge and falling edge of REF_{IN} become active edges at the PFD input.

5-Bit R-Counter

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

12-Bit CLK₁ Divider

Bits DB[14:3] are used to program the CLK₁ divider, which determines the duration of the time step in ramp mode.



NOTES
1. DBB = DOUBLE-BUFFERED BIT(S).

Figure 27. R-Divider Register (R2) Map

10849-022

FUNCTION REGISTER (R3) MAP

With DB[2:0] set to 011, the on-chip function register (Register R3) is programmed as shown in Figure 28.

Reserved Bits

All reserved bits except DB17 must be set to 0 for normal operation.

Negative Bleed Current

DB[24:22] sets the negative bleed current value (I_{BLEED}).

I_{BLEED} should be the closest possible value according to the formula:

$$I_{BLEED} = (4 \times I_{CP}) / N$$

where:

I_{CP} is the charge pump current.

N is the N counter value.

Negative Bleed Enable

When DB21 is set to 0, negative bleed is disabled. When set to 1, negative bleed is enabled. Negative bleed works by adding a constant offset to the charge pump. This has the effect of linearizing the charge pump by moving away from the non-linear area near the origin.

Charge Cancellation

When DB19 is set to 0, charge cancellation is disabled. When set to 1, charge cancellation is enabled.

ABP

When DB17 is set to 0, a wide Anti-Backlash Pulse is used.

When set to 1, a narrow Anti-Backlash Pulse is used.

Loss of Lock (LOL)

This bit enables/disables loss of lock indication. This setting indicates loss of lock even in the case of removing the reference, which is a big advantage over the standard implementation of lock detect.

N SEL

This setting is used to circumvent the issue of pipeline delay between updates of the integer and fractional values in the N-counter. Typically, the INT value is loaded first, followed by the FRAC value. This can cause the N-counter value to be at an incorrect value for a brief period of time equal to the pipeline delay (about four PFD cycles). This has no effect if the INT value has not been updated. However, if the INT value has been changed, this can cause the PLL to overshoot in frequency while it tries to lock to the temporarily incorrect N value. After the correct fractional value is loaded, the PLL quickly locks to the correct frequency. Introducing an additional delay to the loading of the INT value using the N SEL bit causes the INT and

FRAC values to be loaded at the same time, preventing frequency overshoot. The delay is turned on by setting Bit DB15 to 1.

Σ - Δ Reset

For most applications, DB14 should be set to 0. When DB14 is set to 0, the Σ - Δ modulator is reset on each write to Register R0. If it is not required that the Σ - Δ modulator be reset on each Register R0 write, set this bit to 1.

Ramp Mode

DB[11:10] determine the type of generated waveform.

PSK Enable

When DB9 is set to 1, PSK modulation is enabled. When to 0, PSK modulation is disabled. See Phase Shift Keying (PSK) for more information.

FSK Enable

When DB8 is set to 1, FSK modulation is enabled. When set to 0, FSK modulation is disabled. See Frequency Shift Keying (FSK) for more information.

Lock Detect Precision (LDP)

When DB7 is programmed to 0, 24 consecutive PFD cycles of 15 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector (PD) Polarity

DB6 sets the phase detector polarity. When the VCO characteristics are positive, set this bit to 1. When the VCO characteristics are negative, set this bit to 0.

Power-Down

DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock-detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input shift register remains active and capable of loading and latching data.

Charge Pump Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It must be set to 0 for normal operation.

Counter Reset

DB3 is the RF counter reset bit. When this bit is set to 1, the RF synthesizer counters are held in reset. For normal operation, set this bit to 0.

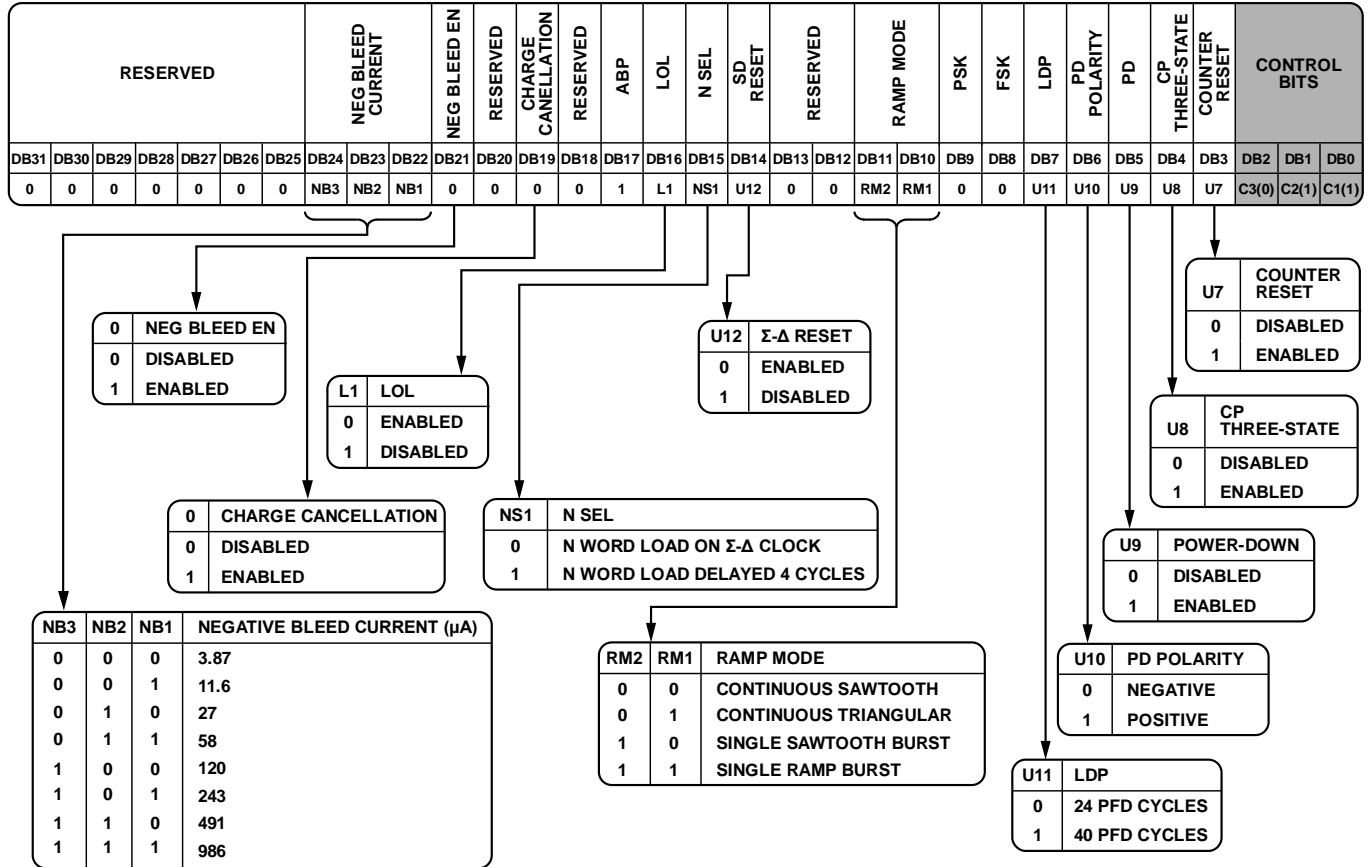


Figure 28. Function Register (R3) Map

10848-023

CLOCK REGISTER (R4) MAP

With DB[2:0] set to 100, the on-chip clock register (Register R4) is programmed as shown in Figure 29.

LE SEL

In some applications, it is necessary to synchronize LE with the reference signal. To do this, DB31 must be set to 1. Synchronization is done internally on the part.

Reserved Bits

All reserved bits must be set to 0 for normal operation.

Ramp Status

DB[22:21] enable or disable the Ramp Status function. *Ramp Complete to MUXOUT* outputs a logic high pulse on MUXOUT at the end of each ramp. *Readback to MUXOUT* allows reading back the synthesizer's frequency at the moment of interruption. See Interrupt Modes and Frequency Readback section for more information.

Clock Divider Mode

Depending on the settings of DB[20:19], the 12-bit clock divider may be a counter for the ramping functions (CLK₂), or it may be turned off.

12-Bit Clock Divider Value

DB[18:7] program the clock divider, which is the CLK₂ timer, while operating in ramp mode. See the Waveform Deviations and Timing section for more details. The timer also determines how long the loop remains in wideband mode while the switched R fast-lock technique is used. See Fast-Lock Timer and Register Sequences for more details.

Clock Divider Select

DB[6] selects which clock divider is loaded with the 12-bit clock divider value. It can be CLK₂ for Ramp 1 or Ramp 2. This is used for fast Ramp, FSK ramp, and dual Ramps. See the Waveform Deviations and Timing section for more details.

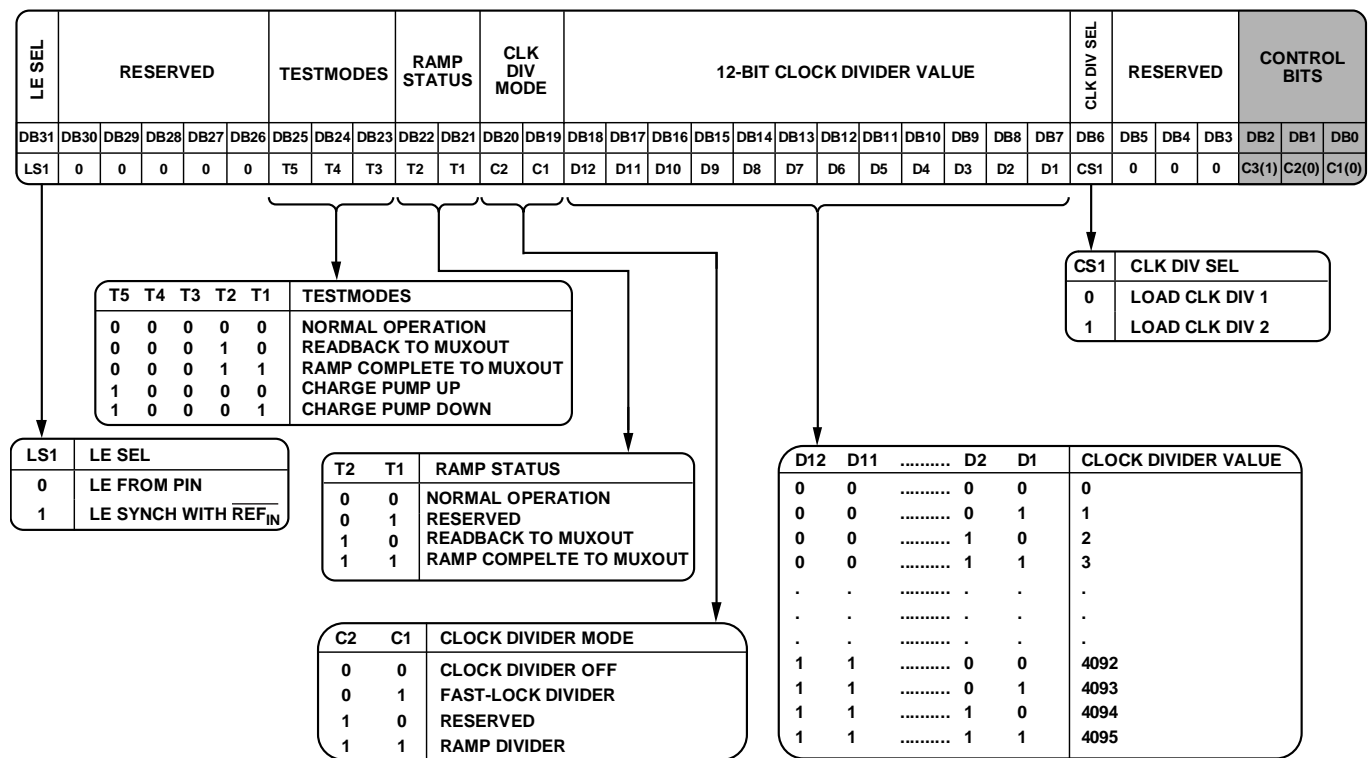


Figure 29. Clock Register (R4) Map

10819-024

DEVIATION REGISTER (R5) MAP

With DB[2:0] set to 101, the on-chip deviation register (Register R5) is programmed as shown in Figure 30.

Reserved Bits

All reserved bits must be set to 0 for normal operation.

TX_{DATA} Invert

With DB30 set to 0, events triggered by TX_{DATA} occur on the rising edge of a TX_{DATA} pulse. When DB30 is set to 1, events triggered by TX_{DATA} occur on the falling edge of a TX_{DATA} pulse.

TX_{DATA} Ramp Clock

Setting DB29 to 0 uses the clock divider clock for clocking the ramp. Setting DB29 to 1 uses the TX_{DATA} clock for clocking the ramp.

PAR Ramp

Setting DB28 to 1 enables the parabolic ramp. Setting DB28 to 0 disables the parabolic ramp. See Nonlinear Ramp Mode.

Interrupt

DB[27:26] determine which type of interrupt is used. This feature is used for reading back the INT and FRAC value of a ramp at a given moment in time (rising edge on the TX_{DATA}

pin triggers the interrupt). From these bits, the frequency can be obtained. After readback, the sweep may continue or stop at the readback frequency.

FSK Ramp Enable

Setting DB25 to 1 enables the FSK ramp. Setting DB25 to 0 disables the FSK ramp.

Ramp 2 Enable

Setting DB24 to 1 enables the second ramp. Setting DB24 to 0 disables the second ramp.

Deviation Select

Setting DB23 to 0 chooses the first deviation word. Setting DB23 to 1, chooses the second deviation word.

4-Bit Deviation Offset Word

DB[22:19] determine the deviation offset. The deviation offset affects the deviation resolution.

16-Bit Deviation Word

DB[18:3] determine the signed deviation word. The deviation word defines the deviation step.

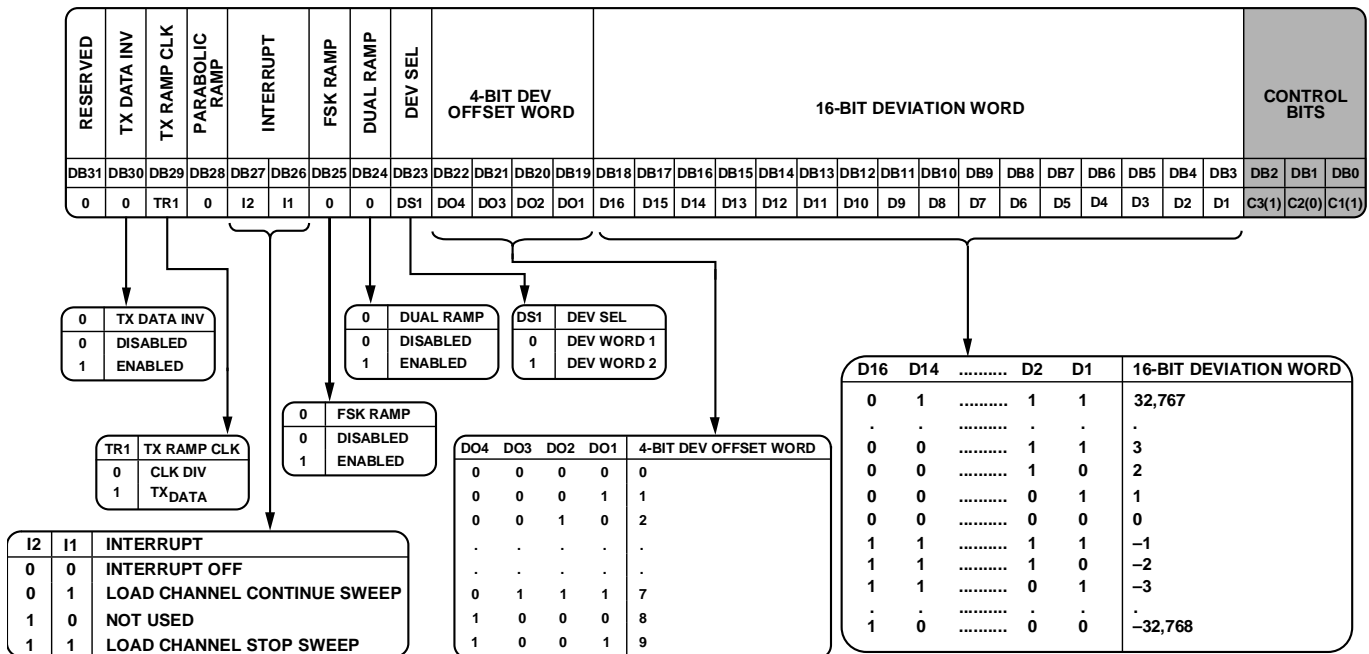


Figure 30. Deviation Register (R5) Map

10849-025

STEP REGISTER (R6) MAP

With DB[2:0] set to 110, the on-chip step register (Register R6) is programmed as shown in Figure 31.

Reserved Bits

All reserved bits must be set to 0 for normal operation.

Step Select

Setting DB23 to 0 chooses Step Word 1. Setting DB23 to 1 chooses Step Word 2.

20-Bit Step Word

DB[22:3] determine the step word. Step word is a number of steps in the ramp.

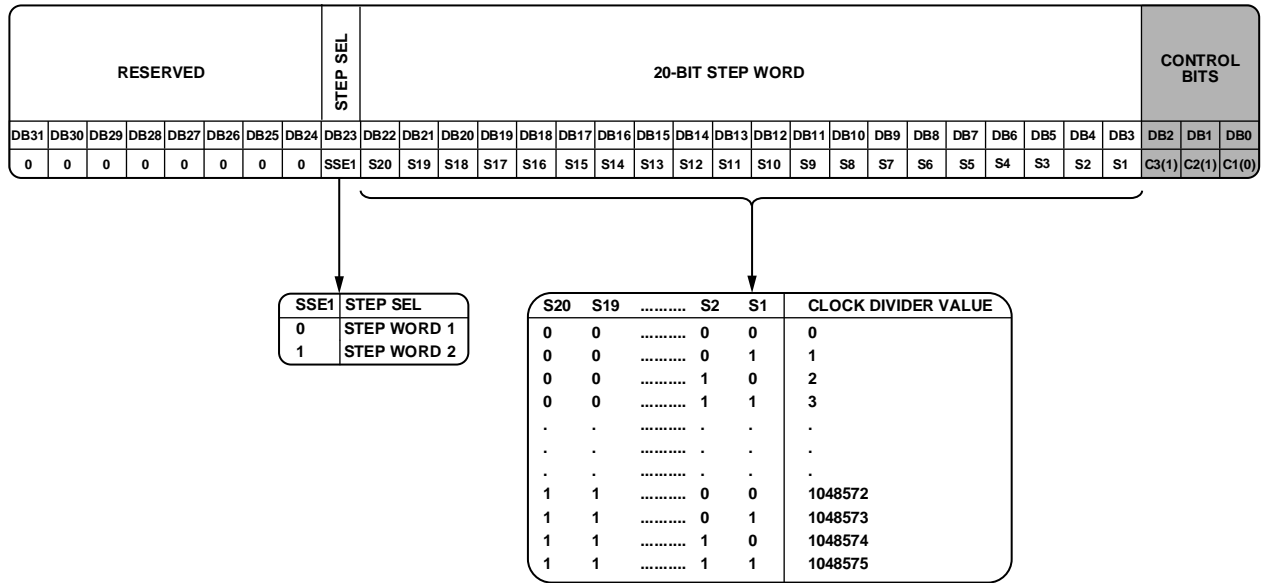


Figure 31. Step Register (R6) Map

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DELAY REGISTER (R7) MAP

With DB[2:0] set to 111, the on-chip delay register (Register R7) is programmed as shown in Figure 32.

Reserved Bits

All reserved bits must be set to 0 for normal operation.

TX_{DATA} Trigger Delay

With DB23 set to 0, there is no delay before that start of the ramp when using TX_{DATA} to trigger a ramp. Setting this bit to 1 means there is a delay, if Delayed Start is enabled.

Triangular Delay

Setting DB22 to 1 enables a delay between each section of a triangular ramp, resulting in a clipped ramp. This setting only works for triangular ramps and when ramp delay is activated. Refer to the Delay Between Ramps section for more details. Setting DB22 to 0 disables the delay between triangular ramps.

Single Full Triangle

Setting DB21 to 1 enables the single full triangle function.

Setting DB21 to 0 disables this function. Refer to the Waveform Generation section for more details.

TX_{DATA} Trigger

If DB20 is set to 1, a logic high on TX_{DATA} activates the ramp.

Setting DB20 to 0 disables this function.

Fast Ramp

Setting DB19 to 1 activates the triangular waveform with two different slopes. It can be used as an alternative to sawtooth ramp because it mitigates the overshoot at the end of the ramp in a waveform. Fast ramp is achieved by changing the top frequency to the bottom frequency in a series of small steps instead of one big step. Setting DB19 to 0 disables this function (see the Ramp Complete Signal to MUXOUT section).

Ramp Delay Fast Lock

Setting DB18 to 1 enables the ramp delay fast lock function. Setting DB10 to 0 disables the function.

Ramp Delay

Setting DB17 to 1 enables the delay between ramps function. Setting DB17 to 0 disables this function.

Delay Clock Select

Setting DB16 to 0 selects the PFD clock as the delay clock. Setting DB16 to 1 selects PFD clock \times CLK₁ (CLK₁ set by DB[14:3] in Register R2) as the delay clock.

Delayed Start Enable

Setting DB15 to 1 enables the delayed start. Setting DB15 to 0 disables the delayed start.

12-Bit Delay Start Word

DB[14:3] determine the delay start word. The delay start word affects the duration of the ramp start delay.

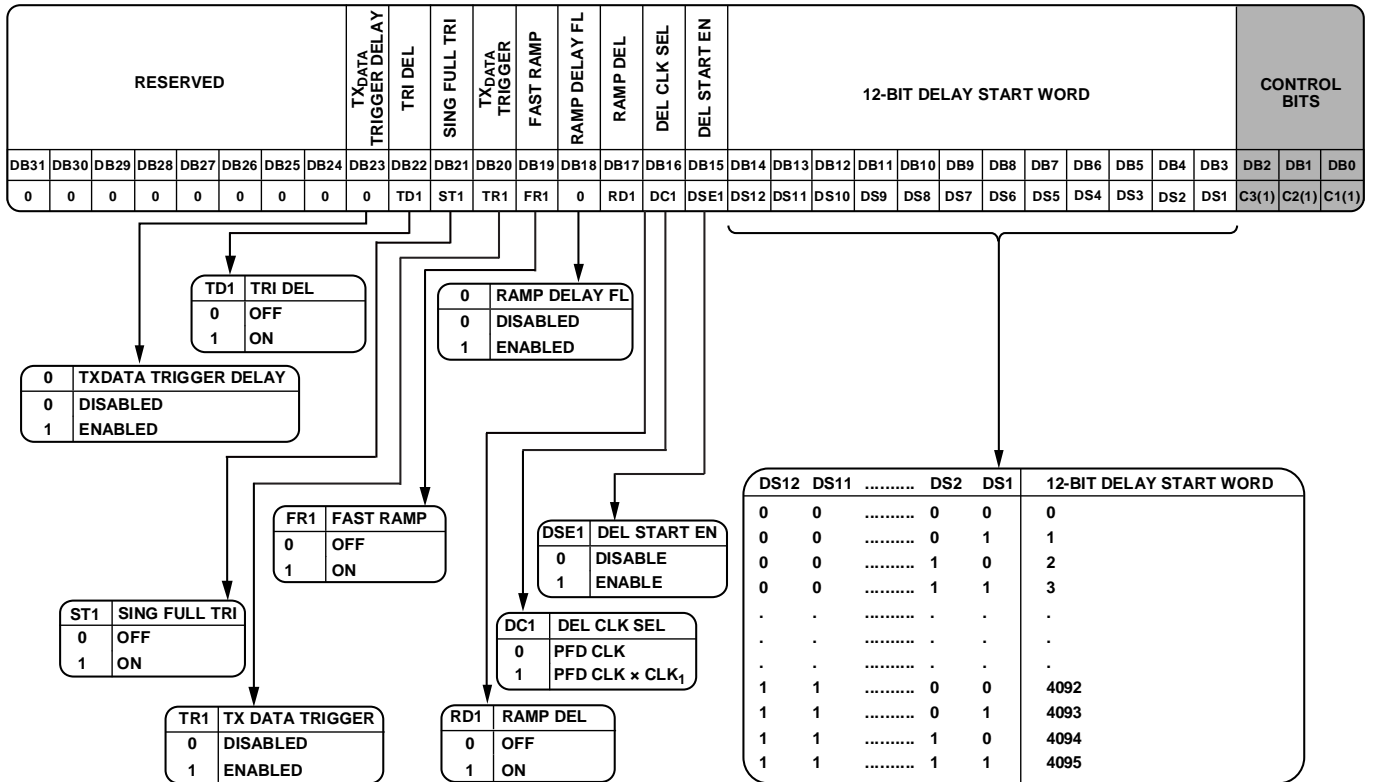


Figure 32. Delay Register (R7) Map

10845027

APPLICATIONS INFORMATION

INITIALIZATION SEQUENCE

After powering up the part, administer the following programming sequence:

1. Delay register (R7)
2. Step register (R6)—load the step register (R6) twice, first with STEP SEL = 0 and then with STEP SEL = 1
3. Deviation register (R5)—load the deviation register (R5) twice, first with DEV SEL = 0 and then with DEV SEL = 1
4. Clock register (R4)—load the clock register (R4) twice, first with CLK DIV SEL = 0 and then with CLK DIV SEL = 1
5. Function register (R3)
6. R-divider register (R2)
7. LSB FRAC register (R1)
8. FRAC/INT register (R0)

RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer must be programmed:

$$RF_{OUT} = [N + (FRAC/2^{25})] \times [f_{PFD}] \quad (4)$$

where:

RF_{OUT} is the RF frequency output.

N is the integer division factor.

$FRAC$ is the fractionality.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (5)$$

where:

REF_{IN} is the reference frequency input.

D is the RF REF_{IN} doubler bit, DB20 in Register R2 (0 or 1).

R is the RF reference division factor.

T is the reference divide-by-2 bit, DB21 in Register R2 (0 or 1).

For example, in a system where a 12.102 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available, the frequency resolution is

$$\begin{aligned} f_{RES} &= REF_{IN}/2^{25} \\ f_{RES} &= 100 \text{ MHz}/2^{25} \\ &= 2.98 \text{ Hz} \end{aligned} \quad (6)$$

From Equation 5,

$$\begin{aligned} f_{PFD} &= [100 \text{ MHz} \times (1 + 0)/1] = 100 \text{ MHz} \\ 12.102 \text{ GHz} &= 100 \text{ MHz} \times (N + FRAC/2^{25}) \end{aligned}$$

Calculating the N and $FRAC$ values,

$$\begin{aligned} N &= \text{int}(RF_{OUT}/f_{PFD}) = 121 \\ FRAC &= F_{MSB} \times 2^{13} + F_{LSB} \\ F_{MSB} &= \text{int}(((RF_{OUT}/f_{PFD}) - N) \times 2^{12}) = 81 \\ F_{LSB} &= \text{int}((((RF_{OUT}/f_{PFD}) - N) \times 2^{12}) - F_{MSB}) \times 2^{13} = \\ &671,088 \end{aligned}$$

where:

F_{MSB} is the 12-bit MSB FRAC value in Register R0.

F_{LSB} is the 13-bit LSB FRAC value in Register R1.

$\text{int}()$ makes an integer of the argument in parentheses.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB.

It is important to note that the PFD cannot be operated above 110 MHz due to a limitation in the speed of the Σ - Δ circuit of the N-divider.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

In fast-locking applications, a wide loop filter bandwidth is required for fast frequency acquisition, resulting in increased integrated phase noise and reduced spur attenuation. Using cycle slip reduction, the loop bandwidth can be kept narrow to reduce integrated phase noise and attenuate spurs while still realizing fast lock times.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared with the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction, slowing down the lock time dramatically. The ADF4159 contains a cycle slip reduction circuit to extend the linear range of the PFD, allowing faster lock times without loop filter changes.

When the ADF4159 detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Stability is main-tained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4159 turns on another charge pump cell. This continues until the ADF4159 detects that the VCO frequency has gone past the desired frequency. It then begins to turn off the extra charge pump cells one by one until they are all turned off and the frequency is settled.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB28 in the R-divider register (Register R2) to 1 enables cycle slip reduction. Note that a 45% to 55% duty cycle is needed on the signal at the PFD in order for CSR to operate correctly. The reference divide-by-2 flip-flop can help to provide a 50% duty cycle at the PFD. For example, if a 100 MHz reference frequency is available and the user wants to run the PFD at 10 MHz, setting the R-divide factor to 10 results in a 10 MHz PFD signal that is not 50% duty cycle. By setting the R-divide factor to 5 and enabling the reference divide-by-2 bit, a 50% duty cycle 10 MHz signal can be achieved.

Note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is negative.

MODULATION

The ADF4159 can operate in frequency shift keying (FSK) or phase shift keying (PSK) mode.

Frequency Shift Keying (FSK)

FSK is implemented by setting the ADF4159 N-divider up for the center frequency and then toggling the TX_{DATA} pin. The deviation from the center frequency is set by

$$f_{DEV} = (f_{PFD} / 2^{25}) \times (DEV \times 2^{DEV_OFFSET}) \quad (7)$$

where:

DEV is a 16-bit word.

DEV_OFFSET is a 4-bit word.

f_{PFD} is the PFD frequency.

The ADF4159 implements this by incrementing or decrementing the set N-divide value by DEV × 2^{DEV_OFFSET}.

Phase Shift Keying (PSK)

When the ADF4159 is set up in PSK mode, output phase of the ADF4159 toggles between 0° and 180°. The TX_{DATA} pin controls the phase.

FSK Settings Worked Example

Take an FSK system operating at 5.8 GHz, with a 25 MHz f_{PFD}, requiring 250 kHz deviation (f_{DEV}).

Rearrange equation 7 as follows:

$$(DEV \times 2^{DEV_OFFSET}) = f_{DEV} / (f_{PFD} / (2^{25}))$$

$$(DEV \times 2^{DEV_OFFSET}) = 250 \text{ kHz} / (25 \text{ MHz} / (2^{25}))$$

$$(DEV \times 2^{DEV_OFFSET}) = 335544.32$$

Let DEV_OFFSET = 6

$$DEV = 335544.32 / (2^6) = 5242.88 \approx 5243$$

Due to rounding of DEV, f_{DEV} = 250.005722 kHz

Toggling the TX_{DATA} pin causes the frequency to hop between ±250 kHz from the programmed center frequency.

WAVEFORM GENERATION

The ADF4159 is capable of generating five types of waveforms in the frequency domain: single ramp burst, single triangular burst, single sawtooth burst, continuous sawtooth ramp, and continuous triangular ramp. Figure 33 through Figure 37 show the types of waveforms available.

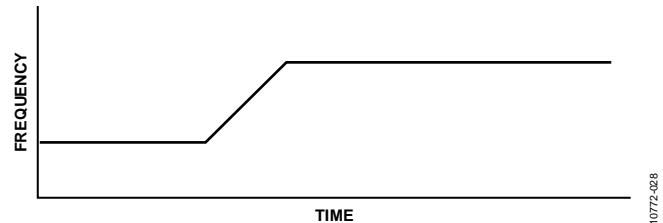


Figure 33. Single Ramp Burst

10772-028

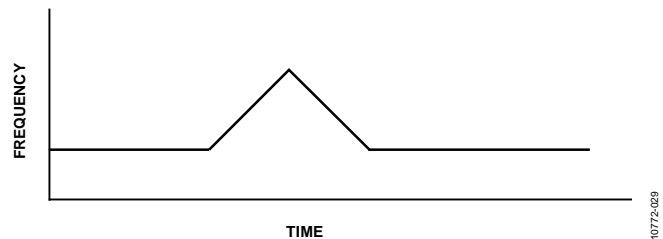


Figure 34. Single Triangular Burst

10772-029

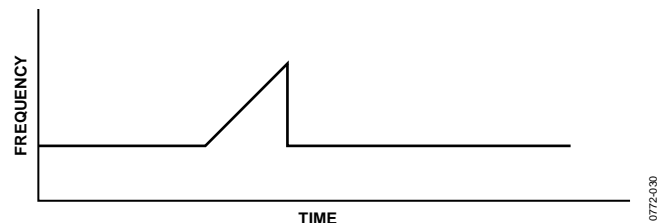


Figure 35. Single Sawtooth Burst

10772-030

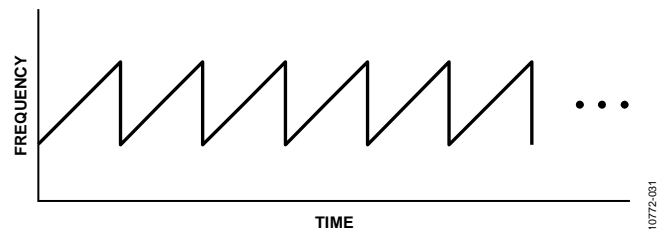


Figure 36. Continuous Sawtooth Ramp

10772-031

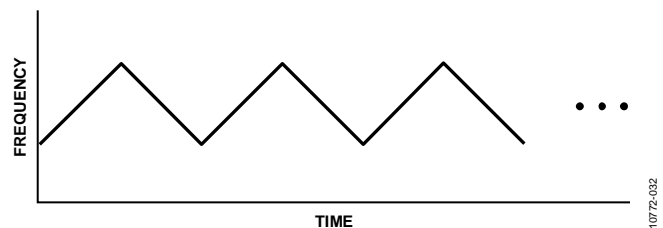


Figure 37. Continuous Triangular Ramp

10772-032

Waveform Deviations and Timing

Figure 38 shows a version of a burst or ramp. The key parameters that define a burst or ramp are

- Frequency deviation
- Timeout interval
- Number of steps

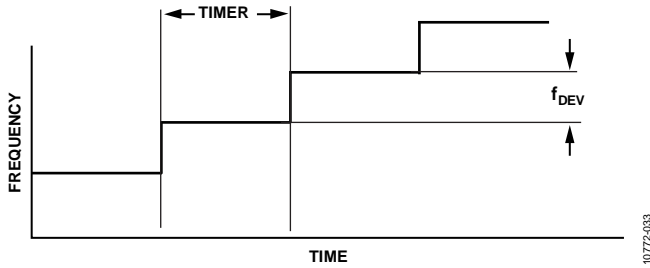


Figure 38. Waveform Timing

Frequency Deviation

The frequency deviation for each frequency hop is set by

$$f_{DEV} = (f_{PFD}/2^{25}) \times (DEV \times 2^{DEV_OFFSET}) \tag{7}$$

where:

DEV is a 16-bit word.

DEV_OFFSET is a 4-bit word.

Timeout Interval

The time between each frequency hop is set by

$$Timer = CLK_1 \times CLK_2 \times (1/f_{PFD}) \tag{8}$$

where:

CLK₁ and *CLK₂* are 12-bit clock values (12-bit *CLK₁* divider in R2 and 12-bit clock divider, DB[20:19] = 11, ramp divider, in Register R4).

f_{PFD} is the PFD frequency.

Number of Steps

A 20-bit step value defines the number of frequency hops that take place. The INT value cannot be incremented by more than 2⁸ = 256 from its starting value.

Single Ramp Burst

The most basic waveform is the single ramp burst. All other waveforms are slight variations of this.

In the single ramp burst, the ADF4159 is locked to the frequency defined in the FRAC/INT register. When the ramp mode is enabled, the ADF4159 increments the N-divide value by DEV × 2^{DEV_OFFSET}, causing a frequency shift, *f_{DEV}*, on each timer interval. This happens until the set number of steps has taken place. The ADF4159 then retains the final N-divide value.

Single Triangular Burst

The triangular burst is similar to the single ramp burst. However, when the steps have been completed, the ADF4159 begins to decrement the N-divide value by DEV × 2^{DEV_OFFSET} on each timeout interval.

Single Sawtooth Burst

In the single sawtooth burst, the N-divide value is reset to its initial value on the next timeout interval after the number of steps has taken place. The ADF4159 retains this N-divide value.

Sawtooth Ramp

The sawtooth ramp is a repeated version of the single sawtooth burst. The waveform repeats until the ramp is disabled.

Triangular Ramp

The triangular ramp is similar to the single ramp burst. However, when the steps have been completed, the ADF4159 begins to decrement the N-divide value by DEV × 2^{DEV_OFFSET} on each timeout interval. When the number of steps has again been completed, it reverts to incrementing the N-divide value. Repeating this creates a triangular waveform. The waveform repeats until the ramp is disabled.

FMCW Radar Ramp Settings Worked Example

Take as an example an FMCW radar system requiring the RF LO to sawtooth ramp over a 50 MHz range every 2 ms. The PFD frequency is 25 MHz, and the RF output range is 5800 MHz to 5850 MHz.

The frequency deviation for each hop in the ramp is set to ~250 kHz.

The frequency resolution of ADF4159 is calculated as follows:

$$f_{RES} = f_{PFD}/2^{25} \tag{9}$$

Numerically,

$$f_{RES} = 25 \text{ MHz}/2^{25} = 0.745 \text{ Hz}$$

The DEV_OFFSET is calculated after rearranging Equation 7:

$$DEV_OFFSET = \log_2(f_{DEV}/(f_{RES} \times DEV_{MAX})) \tag{10}$$

Expressed in log₁₀(x), Equation 10 can be rearranged into the following equation:

$$DEV_OFFSET = \log_{10}(f_{DEV}/(f_{RES} \times DEV_{MAX}))/\log_{10}(2) \tag{11}$$

where:

DEV_{MAX} = 2¹⁵ – Maximum of the Deviation Word.

f_{DEV} is the frequency deviation.

DEV_OFFSET is a 4-bit word.

Using Equation 11, DEV_OFFSET is calculated as follows:

$$DEV_OFFSET = \log_{10}(250 \text{ kHz}/(0.745 \text{ Hz} \times 2^{15}))/\log_{10}(2) = 3.356$$

After rounding, DEV_OFFSET = 4.

From DEV_OFFSET, the resolution of frequency deviation can be calculated as follows:

$$f_{DEV_RES} = f_{RES} \times 2^{DEV_OFFSET} \tag{12}$$

$$f_{DEV_RES} = 0.745 \text{ Hz} \times 2^4 = 11.92 \text{ Hz}$$

To calculate the DEV word, use Equation 10.

$$DEV = f_{DEV} / (f_{RES} \times 2^{DEV_OFFSET}) \tag{13}$$

$$DEV = \frac{250 \text{ kHz}}{\frac{25 \text{ MHz}}{2^{25}} \times 2^4} = 20,971.52$$

Rounding this to 20,972 and recalculating using Equation 7 to obtain the actual deviation frequency, f_{DEV} , thus produces the following:

$$f_{DEV} = (25 \text{ MHz} / 2^{25}) \times (20,972 \times 2^4) = 250.006 \text{ kHz}$$

The number of f_{DEV} steps required to cover the 50 MHz range is $50 \text{ MHz} / 250.006 \text{ kHz} = 200$. To cover the 50 MHz range in 2 ms, the ADF4159 must hop every $2 \text{ ms} / 200 = 10 \mu\text{s}$.

Rearrange Equation 8 to set the timer value (and set CLK_2 to 1):

$$CLK_1 = \text{Timer} \times f_{PFD} / CLK_2 = 10 \mu\text{s} \times 25 \text{ MHz} / 1 = 250$$

To summarize the settings: $DEV = 20,972$, number of steps = 200, $CLK_1 = 250$, $CLK_2 = 1$ ($DB[20:19] = 11$, ramp divider, in Register R4). Using these settings, program the ADF4159 to a center frequency of 5800 MHz, and enable the sawtooth ramp to produce the required waveform. If a triangular ramp is used with the same settings, the ADF4159 sweeps from 5800 MHz to 5850 MHz and back down again, taking 4 ms for the entire sweep.

Activating the Ramp

After setting all of the previous parameters, the ramp must be activated by choosing the desired type of ramp ($DB[11:10]$ in Register R3) and starting the ramp ($DB31 = 1$ in Register R0).

Ramp Programming Sequence

The setting of parameters described in the FMCW Radar Ramp Settings Worked Example section and the activation of the ramp described in the Activating the Ramp section must be completed in the following register write order:

1. Delay register (R7)
2. Step register (R6)
3. Deviation register (R5)
4. Clock register (R4)
5. Function register (R3)
6. R-divider register (R2)
7. LSB FRAC register (R1)
8. FRAC/INT register (R0)

OTHER WAVEFORMS

Two Ramp Rates

This feature allows for two ramps with different step and deviation settings. It also allows the ramp rate to be reprogrammed while another ramp is running.

Example

For example, if

- PLL is locked to 5790 MHz and $f_{PFD} = 25\text{MHz}$.
- Ramp 1 jumps 100 steps, each of which lasts $10 \mu\text{s}$ and has a frequency deviation of 100 kHz.
- Ramp 2 jumps 80 steps, each of which lasts $10 \mu\text{s}$ and has a frequency deviation of 125 kHz.

Then,

1. $DB24$ in Register R5 must be set to 1, which activates Ramp 2 rates mode.
2. Program Ramp 1 and Ramp 2 as follows to get two ramp rates:

Ramp 1:

- a. Register R5 with $DB23 = 0$:
 - i. $DB[18:3] = 16,777$
 - ii. $DB[22:19] = 3$
- b. Register R6 with $DB23 = 0$:
 - i. $DB[22:3] = 100$

1. Ramp 2:

- a. Register R5 with $DB23 = 1$:
 - i. $DB[18:3] = 20,972$
 - ii. $DB[22:19] = 3$
- b. Register R6 with $DB23 = 1$:
 - i. $DB[22:3] = 80$

The resulting ramp with two various rates is shown in Figure 39. Eventually, the ramp must be activated as described in Activating the Ramp section.

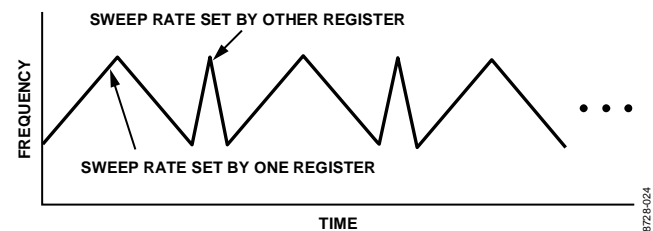


Figure 39. Dual Sweep Rate

Ramp Mode with FSK Signal on Ramp

In traditional approaches a FMCW radars used either linear frequency modulation (LFM) or FSK modulation. These modulations used separately introduce ambiguity between measured distance and velocity, especially in multitarget situations. To overcome this issue and enable unambiguous (range – velocity) multitarget detection, use a ramp with FSK on it.

Example

For example, if

- PLL is locked to 5790 MHz and $f_{PFD} = 25\text{MHz}$.
- There are 100 steps each of which lasts $10 \mu\text{s}$ and has a deviation of 100 kHz.
- The FSK signal is 25 kHz.

Then,

1. Program the ramp as described in the FMCW Radar Ramp Settings Worked Example section. While doing that DB23 in Register R5 and DB23 in Register R6 must be set to 0.
2. Set the bits in Register R5 as follows to program FSK on ramp to 25 kHz:
 - a. DB[18:3] = 4194 (deviation word)
 - b. DB[22:19] = 3 (deviation offset)
 - c. DB23 = 1 (deviation select for FSK on ramp)
 - d. DB25 = 1 (ramp with FSK enabled).

An example of ramp with FSK on the top of it is shown in Figure 40. Eventually, the ramp must be activated as described in the Activating the Ramp section.

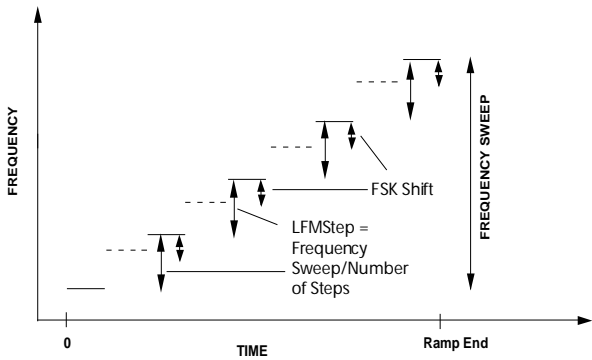


Figure 40. Combined FSK and LFM Waveform (N Corresponds to the Number of LFM Steps)

Delayed Start

A delayed start can be used with two different parts to control the start time. The theory of delayed start is shown in Figure 41.

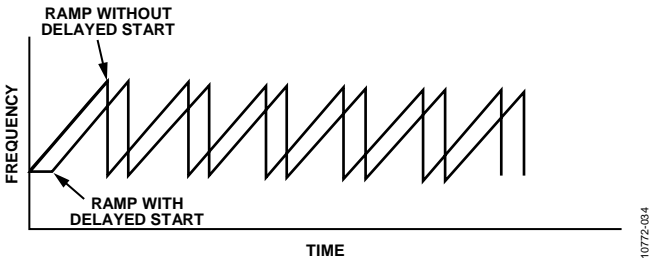


Figure 41. Delayed Start of Sawtooth Ramp

Example

For example, to program a delayed start with two different parts to control the start time,

1. Set DB15 in Register R7 to 1 to enable the delayed start of ramp option.
2. Set Bit DB16 in Register R7 to 0 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp on

the first part by 5 μ s. $f_{PFDD} = 25$ MHz. The delay is calculated as follows:

$$\begin{aligned} \text{Delay} &= t_{PFDD} \times \text{Delay Start Word} \\ &= 40 \text{ ns} \times 125 = 5 \mu\text{s} \end{aligned}$$

3. Set Bit DB16 in Register R7 to 1 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp on the second part by 125 μ s. Use the following formula for calculating the delay:

$$\begin{aligned} \text{Delay} &= t_{PFDD} \times CLK_1 \times \text{Delay Start Word} \\ &= 40 \text{ ns} \times 25 \times 125 = 125 \mu\text{s} \end{aligned}$$

Eventually, the ramp must be activated as described in the Activating the Ramp section.

Delay Between Ramps

This feature adds a delay between bursts in ramp. Figure 42, Figure 43, and Figure 44 show a delay between ramps in sawtooth, triangular, and clipped triangular mode, respectively.

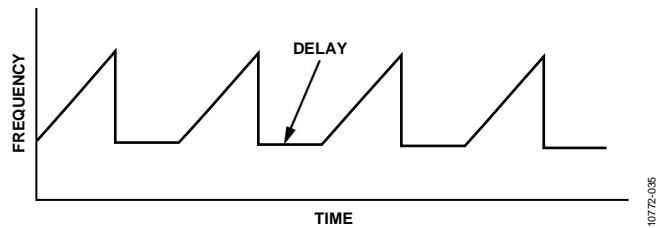


Figure 42. Delay Between Ramps for Sawtooth Mode

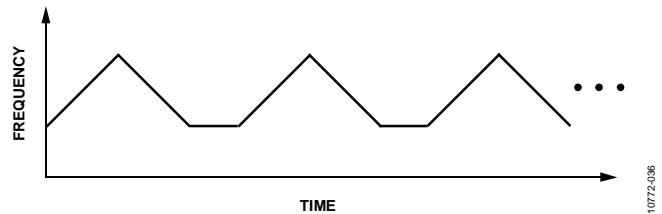


Figure 43. Delay Between Ramps for Triangular Mode

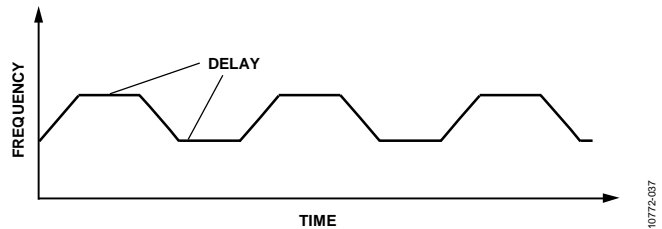


Figure 44. Delay Between Ramps for Clipped Triangular Mode

Example

For example, to add a delay between bursts in a ramp,

1. Set DB17 in Register R7 to 1 to enable the delay between ramps option.
2. Set Bit DB16 in Register R7 to 0 and the 12-bit delay start word (DB[14:3] in Register R7) to 125 to delay the ramp by 5 μ s. $f_{PFDD} = 25$ MHz. The delay is calculated as follows:

$$\begin{aligned} \text{Delay} &= t_{\text{PFD}} \times \text{Delay Start Word} \\ &= 40 \text{ ns} \times 125 = 5 \mu\text{s} \end{aligned}$$

If a longer delay is needed, for example, 125 μs, set Bit DB16 in Register R7 to 1 and the 12-bit delay start word (DB[14:3] in Register R7) to 125. The delay is calculated as follows:

$$\begin{aligned} \text{Delay} &= t_{\text{PFD}} \times \text{CLK}_1 \times \text{Delay Start Word} \\ &= 40 \text{ ns} \times 25 \times 125 = 125 \mu\text{s} \end{aligned}$$

There is also a possibility to activate fast-lock operation for the first period of delay. This is done by setting Bit DB18 in Register R7 to 1. This feature is useful for sawtooth ramps to mitigate the frequency overshoot on the transition from one sawtooth to the next. Eventually, the ramp must be activated as described in Activating the Ramp section.

Two Ramp Rates Mode with Delay

This mode combines the Two Ramp Rates with Delay Between Ramps.

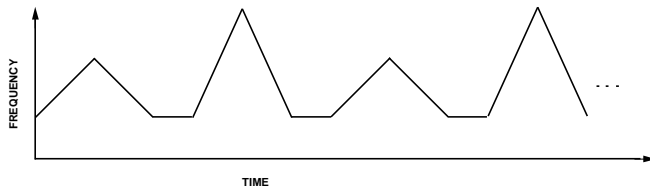


Figure 45 Two Ramp Rates Mode with Delay

First the Two Ramp Rates must be programmed as described in the Example in Two Ramp Rates section and then the delay must be programmed as described in Delay Between Ramps Section on Page 27.

Nonlinear Ramp Mode

The ADF4159 is capable of generating a parabolic ramp. The output frequency is generated according to the following equation:

$$f_{\text{OUT}}(n + 1) = f_{\text{OUT}}(n) + n \times f_{\text{DEV}} \tag{16}$$

where:

- f_{OUT} is output frequency.
- f_{DEV} is frequency deviation.
- n is step number.

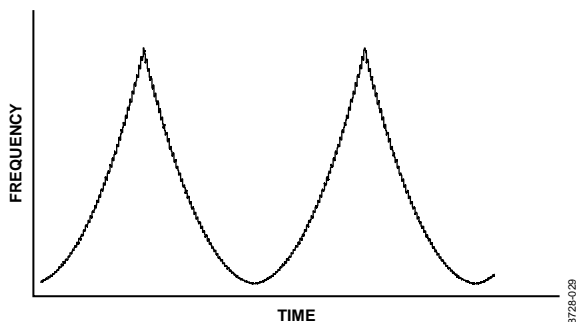


Figure 46. Parabolic Ramp

The following example explains how to set up and use this function.

Example

$$f_{\text{OUT}} = 5790 \text{ MHz}$$

$$f_{\text{DEV}} = 100 \text{ kHz}$$

Number of steps = 50

Duration of a single step = 10 μs

Ramp mode must be either continuous triangular (Register R3, DB[11:10] = 01) or single ramp burst (Register R3, DB[11:10] = 11) or single triangular burst (Register R3, DB[11:10] = 11 and Register R7, DB21 = 1).

In the first case, the generated frequency range is calculated as follows:

$$\begin{aligned} \Delta f &= f_{\text{DEV}} \times (\text{Number of Steps} + 2) \times (\text{Number of Steps} + 1)/2 \\ &= 132.6 \text{ MHz} \end{aligned}$$

In the second case, the generated frequency range is calculated as follows:

$$\begin{aligned} \Delta f &= f_{\text{DEV}} \times (\text{Number of Steps} + 1) \times \text{Number of Steps}/2 \\ &= 127.5 \text{ MHz} \end{aligned}$$

The timer is set in the same way as for its linear ramps described in the Waveform Generation section on Page 24.

Activation of the parabolic ramp is achieved by setting Bit DB28 in Register R5 to 1.

Next the counter reset (DB3 in Register R3) must be set first to 1 and then to 0.

Eventually, the ramp must be activated as described in the Activating the Ramp section on Page 25.

Fast Ramp Mode

The ADF4159 is capable of generating a fast ramp.

The fast ramp is a triangular ramp with two different slopes. Figure 47 shows the fast ramp. The number of steps, time per step and deviation per step is programmable for both the up and down ramp.

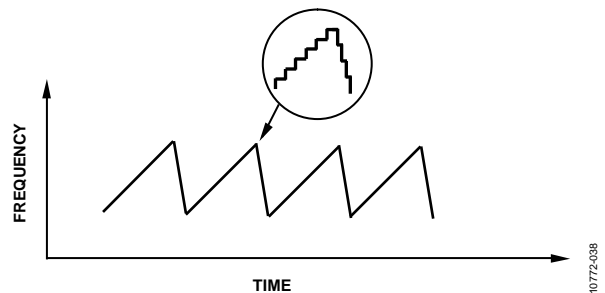


Figure 47. Fast Ramp Mode

To activate this waveform:

1. Select the continuous waveform by setting DB[11:10] = 0b01 in Register R3.
2. Select Fast Ramp enable by setting DB19 = 0b1 in Register R7.
3. Program the 'up' ramp:
 - a. Set CLK DIV SEL (R4, DB6), DEV SEL (R5, DB23) and STEP SEL (R6, DB23) to **0b0** for Ramp 1.
 - b. Calculate and program the timer, DEV, DEV_OFFSET and step word as described in FMCW Radar Ramp Settings Worked Example.
4. Program the 'down' ramp:
 - a. Set CLK DIV SEL (R4, DB6), DEV SEL (R5, DB23) and STEP SEL (R6, DB23) to **0b1** for Ramp 2.
 - b. Calculate and program the timer, DEV, DEV_OFFSET and step word as described in step 3.
5. Start the ramp by setting DB31 = 0b1 in Register R0.

Note that the total frequency change of the 'up' and 'down' ramps must be equal for stability.

Ramp Complete Signal to MUXOUT

The ramp complete signal on MUXOUT is shown in Figure 48.

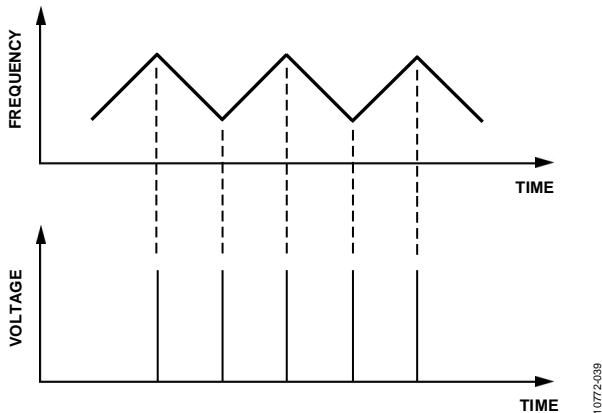


Figure 48. Ramp Complete Signal on MUXOUT

To activate this function, set DB[30:27] = 1111 in Register R0 and DB[25:21] = 00011 in Register R4.

Interrupt Modes and Frequency Readback

Interrupt modes are triggered from the rising edge of TX_{DATA}. Depending on the settings of DB[27:26] in Register R5, the modes in Table 7 are activated.

Table 7. Interrupt Modes

| Mode | Action |
|------|--------|
|------|--------|

| | |
|----------------|---|
| DB[27:26] = 00 | Interrupt is off |
| DB[27:26] = 01 | Interrupt on TX _{DATA} , sweep continues |
| DB[27:26] = 11 | Interrupt on TX _{DATA} , sweep stops |

When an interrupt takes place, the data consisting of the INT and FRAC values can be read back via MUXOUT. The data is made up of 37 bits, 12 of which represent the INT value and 25 the FRAC value.

The theory of frequency readback is illustrated in Figure 49.

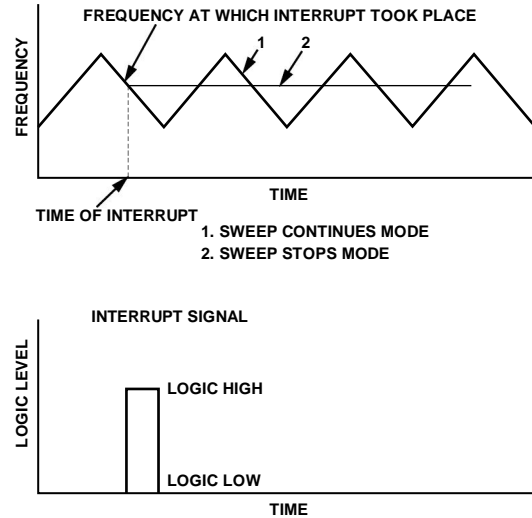
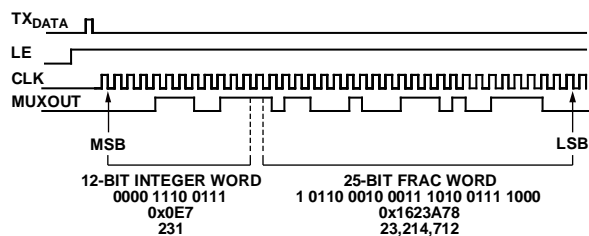


Figure 49. Interrupt and Frequency Readback

Note that DB[22:21] in Register R4 must be set to 0b10 and DB[30:27] in Register R0 (MUXOUT control) must be set to 0b1111.

The mechanism of how single bits are read back is shown in Figure 50.

DATA CLOCKED OUT ON POSITIVE EDGE OF CLK AND READ ON NEGATIVE EDGE OF CLK READBACK WORD (37 BITS)
 0 0001 1100 1111 0110 0010 0011 1010 0111 1000 (0x1CF623A78)



$$RF = f_{\text{PFD}} \times (231 + 23214712/2^{25}) = 1.7922963\text{GHz}$$

Figure 50. Reading Back Single Bits to Determine the Output Frequency at the Moment of Interrupt

For continuous frequency readback, the following sequence must be used:

2. Register 0 write
3. LE high
4. Pulse on TX_{DATA}

- 5. Frequency readback (as described at the beginning of the Interrupt Modes and Frequency Readback section and Figure 50)
- 6. Pulse on TX_{DATA}
- 7. Register R4 write

- 8. Frequency readback (as described at the beginning of the Interrupt Modes and Frequency Readback section and Figure 50)
- 9. Pulse on TX_{DATA}

The sequence is also shown in Figure 51.

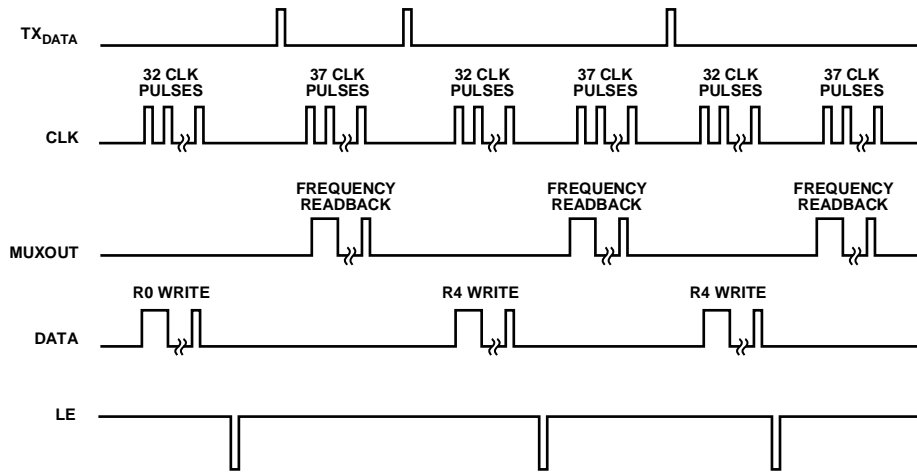


Figure 51. Continuous Frequency Readback

10772-042

FAST LOCK MODE

ADF4159 can operate in fast lock mode. In this mode charge pump current is boosted and additional resistors are connected to maintain the stability of the loop.

Fast-Lock Timer and Register Sequences

If the fast-lock mode is used, a timer value needs to be loaded into the PLL to determine the time spent in wide bandwidth mode.

When the DB[20:19] bits in Register 4 (R4) are set to 01 (fast-lock divider), the timer value is loaded via the 12-bit clock divider value. To use fast lock, the PLL must be written to in the following sequence:

1. Initialization sequence (see the Initialization Sequence section on Page 23). This must be performed once after powering up the part.
2. Load Register R4 DB[20:19] = 01 and the chosen fast-lock timer value (DB[18:7]).
3. Load Register R2 with the chosen CLK₁ divider value (DB[14:3]) if longer time in wide loop bandwidth is required.

Note that the duration that the PLL remains in wide bandwidth is equal to the CLK₁ × fast-lock timer / f_{PFD}, where CLK₁ is the 12-bit CLK₁ divider in Register R2.

Note that the fast-lock feature doesn't work in ramp mode.

Fast Lock: An Example

If a PLL has a reference frequency of 13 MHz, that is, f_{PFD} = 13 MHz, as well as CLK₁ = 10 (12-bit CLK₁ divider in Register R2) and a required lock time of 50 μs, the PLL is set to wide bandwidth for 40 μs.

If the time period set for the wide bandwidth is 40 μs, then

$$\text{Fast-Lock Timer Value} = \text{Time in Wide Bandwidth} \times f_{\text{PFD}} / \text{CLK}_1$$

$$\text{Fast-Lock Timer Value} = 40 \mu\text{s} \times 13 \text{ MHz} / 10 = 52.$$

Therefore, 52 must be loaded into the clock divider value in Register R4 in Step 2 of the sequence described in the Fast-Lock Timer and Register Sequences section on Page 30.

Fast Lock: Loop Filter Topology

To use fast-lock mode, an extra connection from the PLL to the loop filter is needed. The damping resistor in the loop filter must be reduced to ¼ of its value while in wide bandwidth mode. This is required because the charge pump current is increased by 16 while in wide bandwidth mode, and stability must be ensured. To further enhance stability and mitigate frequency overshoot while frequency change (in wide bandwidth mode), Resistor R3 is connected. During fast lock, the SW1 pin is shorted to ground and SW2 is connected to CP (it

is done by setting Bits DB[20:19] in Register R4 to 01—fast lock divider). The following two topologies can be used:

- Divide the damping resistor (R1) into two values (R1 and R1A) that have a ratio of 1:3 (see Figure 52).
- Connect an extra resistor (R1A) directly from SW1, as shown in Figure 53. The extra resistor must be chosen such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to ¼ of the original value of R1.

For both of the topologies, the ratio R3:R2 must equal 1:4.

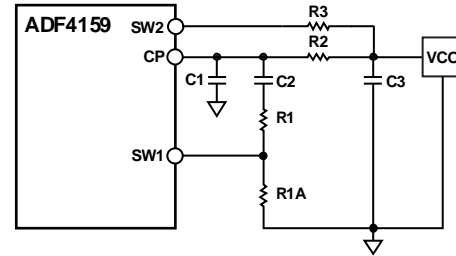


Figure 52. Fast-Lock Loop Filter Topology—Topology 1

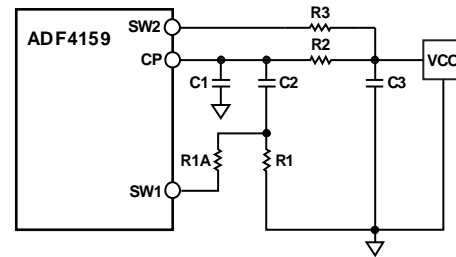


Figure 53. Fast-Lock Loop Filter Topology—Topology 2

SPUR MECHANISMS

The fractional interpolator in the ADF4159 is a third-order Σ-Δ modulator (SDM) with a 25-bit fixed modulus (MOD). The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/CLK₁. The various spur mechanisms possible with fractional-N synthesizers and how they affect the ADF4159 are described in this section.

Fractional Spurs

In most fractional synthesizers, fractional spurs can appear at the set channel spacing of the synthesizer. In the ADF4159, these spurs do not appear. The high value of the fixed modulus in the ADF4159 makes the SDM quantization error spectrum look like broadband noise, effectively spreading the fractional spurs into noise.

Integer Boundary Spurs

Interactions between the RF VCO frequency and the PFD frequency can lead to spurs known as integer boundary spurs. When these frequencies are not integer related (which is the purpose of the fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that

corresponds to the beat note or difference frequency between an integer multiple of the PFD and the VCO frequency.

These spurs are named integer boundary spurs because they are more noticeable on channels close to integer multiples of the PFD where the difference frequency can be inside the loop bandwidth. These spurs are attenuated by the loop filter on channels far from integer multiples of the PFD.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is the feedthrough of low levels of on-chip reference switching noise out through the RF_{IN}x pins back to the VCO, resulting in reference spur levels as high as -90 dBc. Take care in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

Low Frequency Applications

The specification on the RF input is 0.5 GHz minimum; however, RF frequencies lower than this can be used if the minimum slew rate specification of 400 V/μs is met. An appropriate driver can be used to accelerate the edge transitions of the RF signal before it is fed back to the ADF4159 RF input. The ADCMP553 is one such driver.

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user implement PLL design. Visit www.analog.com/pll to download the free ADIsimPLL™ software. This software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

PCB DESIGN GUIDELINES FOR THE CHIP SCALE PACKAGE

The lands on the chip scale package (CP-24) are rectangular. The printed circuit board (PCB) pad for these must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the PCB must be at least as large as this exposed pad. On the PCB, there must be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, incorporate them into the thermal pad at the 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 ounce of copper to plug the via. Connect the PCB thermal pad to AGND.

APPLICATION OF ADF4159 IN FMCW RADAR

The application of the ADF4159 in a FMCW radar system is shown in Figure 54. The ADF4159 in a FMCW radar is used for generating ramps (sawtooth or triangle) that are necessary for this type of radar to operate. Traditionally, the PLL was driven directly by a direct digital synthesizer (DDS) to generate the required type of waveform. Due to the implemented waveform generating mechanism on the ADF4159, a DDS is no longer

needed, which reduces cost. In addition, the PLL solution has advantages over another method (the DAC driving the VCO directly) for generating FMCW ramps, which suffered from nonlinearities of the VCO tuning characteristics requiring compensation. The PLL method produces highly linear ramps without the need for calibration.

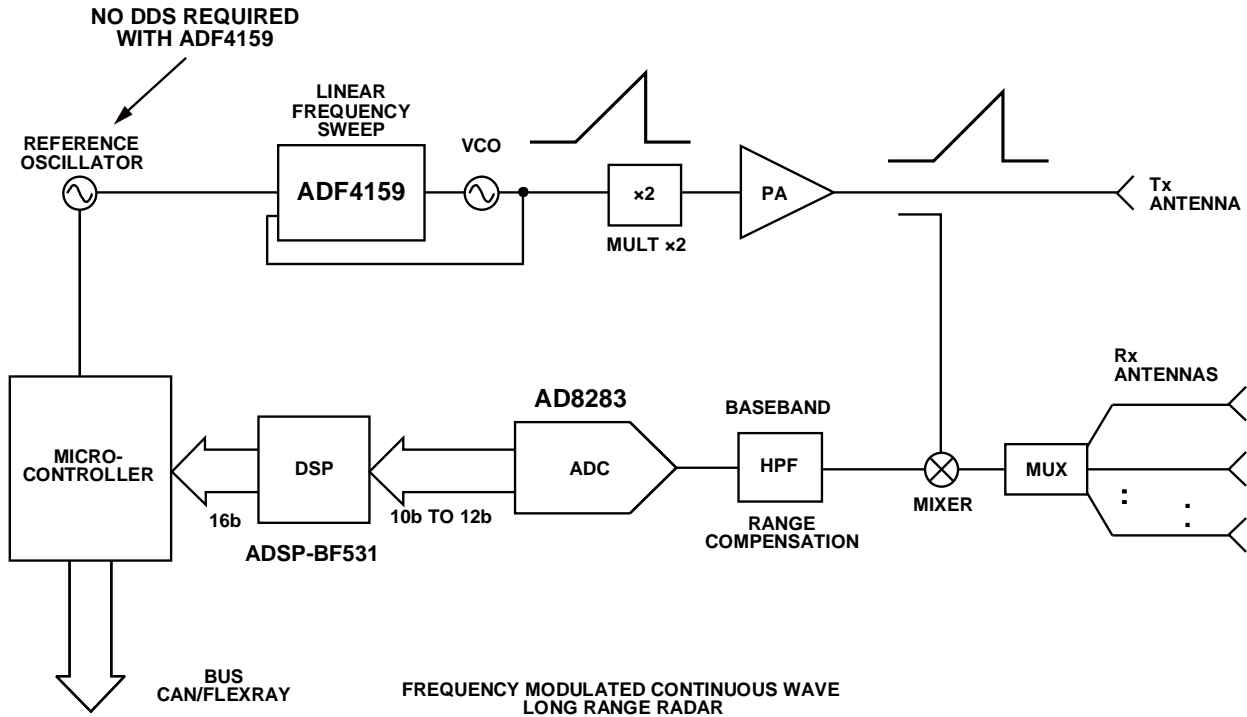
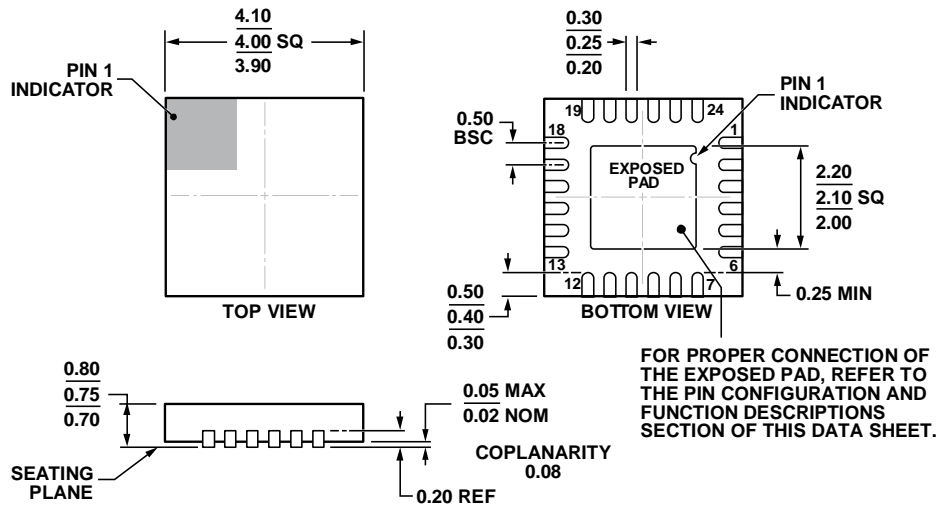


Figure 54. FMCW Radar with ADF4159

10845-043

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 55. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 4 mm × 4 mm Body, Very Very Thin Quad
 (CP-24-7)
 Dimensions shown in millimeters

06-11-2012-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| ADF4159CCPZ | -40°C to +125°C | 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-24-7 |
| ADF4159CCPZ-RL7 | -40°C to +125°C | 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-24-7 |
| ADF4159WCCPZ | -40°C to +125°C | 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-24-7 |
| ADF4159WCCPZ-RL7 | -40°C to +125°C | 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-24-7 |

¹ Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).